# NAVAL POSTGRADUATE SCHOOL
# MONTEREY, CALIFORNIA

DTIC QUALITY INSPECTED 4

# THESIS

ANALYSIS, SIMULATION AND  DESIGN OF
THE MAPHAM CONVERTER

by

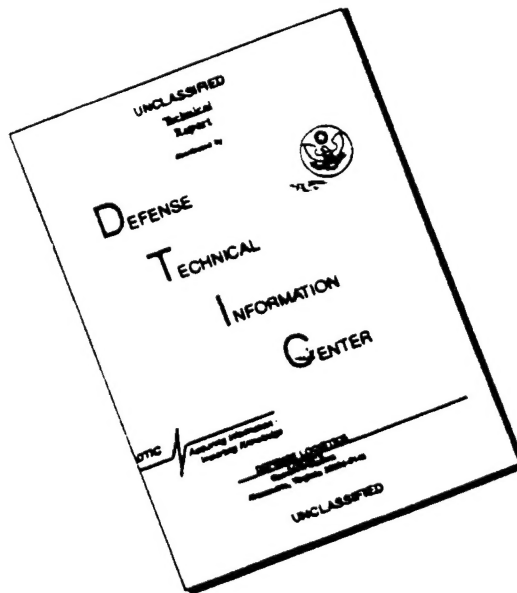Jerry D. Tyner

December, 1995

Thesis Advisor: John G. Ciezki

19960328 014

# DISCLAIMER NOTICE



THIS DOCUMENT IS BEST
QUALITY AVAILABLE. THE COPY
FURNISHED TO DTIC CONTAINED
A SIGNIFICANT NUMBER OF
PAGES WHICH DO NOT
REPRODUCE LEGIBLY.

| REPORT DOCUMENTATION PAGE | | | Form Approved OMB No. 0704-0188 |
|---|---|---|---|

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503.

| 1. AGENCY USE ONLY *(Leave blank)* | 2. REPORT DATE December 1995 | 3. REPORT TYPE AND DATES COVERED Master's Thesis |
|---|---|---|

| 4. TITLE AND SUBTITLE  ANALYSIS, SIMULATION AND DESIGN OF THE MAPHAM CONVERTER | 5. FUNDING NUMBERS |
|---|---|

| 6. AUTHOR(S)  Tyner, Jerry D. |
|---|

| 7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey CA 93943-5000 | 8. PERFORMING ORGANIZATION REPORT NUMBER |
|---|---|

| 9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) | 10. SPONSORING/MONITORING AGENCY REPORT NUMBER |
|---|---|

| 11. SUPPLEMENTARY NOTES  The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government. |
|---|

| 12a. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution is unlimited. | 12b. DISTRIBUTION CODE |
|---|---|

13. ABSTRACT *(maximum 200 words)*

In the mid to late sixties, Dr. Neville Mapham worked extensively as an application engineer in the Semiconductor Products Department of the General Electric Company, where he specialized in inverters and the high-frequency operation of silicon controlled rectifiers. His success in the power electronics field produced three equivalent parallel output resonant converter configurations, the center-tapped supply, the bridge, and the center-tapped load. To further expand on Dr. Mapham's work, this thesis simulates, analyzes, and designs the center-tapped supply and bridge topologies. Simulation of both configurations is conducted utilizing PSpice software. In addition, the center-tapped supply converter is constructed and studied in the Power Systems Laboratory. For design purposes, a specific listing of hardware components is given. Series connection through a transformer of the Mapham bridge is investigated and implementation issues are addressed.

| 14. SUBJECT TERMS  PSpice simulation, thyristors, silicon controlled rectifiers, resonant converters | 15. NUMBER OF PAGES  82 |
|---|---|
| | 16. PRICE CODE |

| 17. SECURITY CLASSIFICATION OF REPORT Unclassified | 18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified | 19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified | 20. LIMITATION OF ABSTRACT UL |
|---|---|---|---|

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)

Prescribed by ANSI Std. 239-18 298-102

ANALYSIS, SIMULATION AND DESIGN OF THE MAPHAM CONVERTER

Jerry D. Tyner
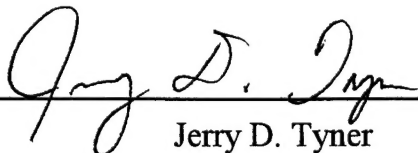Lieutenant, United States Navy
B.S., United States Naval Academy, 1987

Submitted in partial fulfillment
of the requirements for the degree of
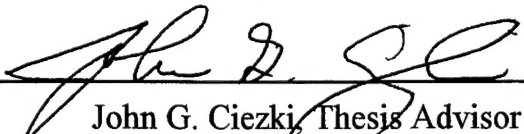
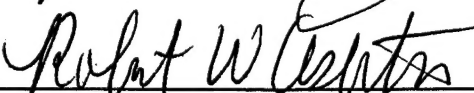**MASTER OF SCIENCE IN ELECTRICAL ENGINEERING**

from the

**NAVAL POSTGRADUATE SCHOOL**
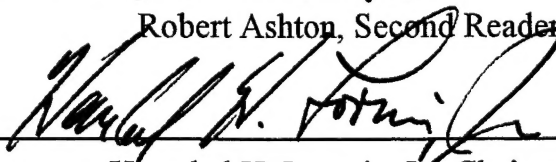**December, 1995**

Author: _____

Jerry D. Tyner

Approved by: _____

John G. Ciezki, Thesis Advisor

_____

Robert Ashton, Second Reader

_____

Herschel H. Loomis, Jr., Chairman
Department of Electrical and Computer Engineering

iii

iv

# ABSTRACT

In the mid to late sixties, Dr. Neville Mapham worked extensively as an application engineer in the Semiconductor Products Department of the General Electric Company, where he specialized in inverters and the high-frequency operation of silicon controlled rectifiers. His success in the power electronics field produced three equivalent parallel output resonant converter configurations, the center-tapped supply, the bridge, and the center-tapped load. To further expand on Dr. Mapham's work, this thesis analyzes, simulates, and designs the center-tapped supply and bridge topologies. Simulation of both configurations is conducted utilizing PSpice software. In addition, the center-tapped supply converter is constructed and studied in the Power Systems Laboratory. For design purposes, a specific listing of hardware components is given. Series connection through a transformer of the Mapham bridge is investigated and implementation issues are addressed.

# TABLE OF CONTENTS

# I. INTRODUCTION

## A. BACKGROUND

A unique type of resonant converter was researched by Dr. Mapham in the late 1960s. His converter combined the good features of all of the prior resonant circuits. These features included reduction of SCR switching losses, absence of SCR misfiring, and increased sensitivity to reactive loads. In order to enhance dc-to-ac converter capability, Dr. Mapham aspired to analyze SCR converter circuits which operate from about 1 kHz up to the then present-day SCR capability of 30 kHz. [Ref. 1]

## B. RESEARCH OBJECTIVES

The main purpose of the research is to identify the capabilities and limitations of a parallel output resonant converter herein referred to as the Mapham converter. Most of today's Department of Defense (DoD) systems must be designed to be smaller, lighter, less expensive, and more reliable. Due to its high-frequency switching (up to 30 kHz) and zero switching losses, the Mapham converter is capable of satisfying all of these objectives. Such converters will hopefully provide a new approach to reducing the weight, size and cost of many DoD systems (i.e. the advanced launch vehicle that was proposed and is currently under construction by NASA.)

1

The tasks considered in this research effort include: 1) developing an analytical representation for the Mapham converter, 2) implementing a digital representation of the Mapham converter using PSpice computer simulations, 3) selecting and acquiring hardware components from design specifications, 4) building a test bed in the Power Systems Laboratory, and 5) re-engineering the computer simulation, if required, to better represent the lab results.

## C. STRUCTURE

This thesis consists of seven parts: Introduction, General Description Of The Mapham Converter, Component Selection, PSpice Simulation, Hardware Implementation, Series Connection Of Converter Through A Transformer, and Conclusion.

In the second chapter, "General Description Of The Mapham Converter," the background and characteristics of the Mapham converter are introduced. Also, a representative topology is analyzed, emphasizing a discussion on current conduction, gating pulses, and the resonant frequency.

The "Component Selection" chapter contains an explanation of how the circuit elements L, C, and R are determined. A complete picture is given for the design procedure, including the specifications for the silicon controlled rectifier (SCR), the diode, and all other general specifications. Utilization of the term SCR and thyristor is interchangeable.

In the "PSpice Simulation" chapter a thorough overview of the PSpice software is provided. Its set-up, version used, along with the capabilities and limitations of each version, are discussed. The results of the simulation of the Mapham converter at various frequencies are reviewed fully.

The "Hardware Implementation" chapter includes a description of the actual components used in the Power Systems Laboratory. The part description and specifications for each component is provided, along with the implementation issues discovered when conducting the research.

In the "Series-Connected Mapham Converter Through A Transformer" chapter, the circuit topology and its operation are discussed. In addition, results from PSpice simulation, network studies and future research are addressed.

In the concluding chapter, the objectives are contrasted with the successes and failures of the research endeavor. Extensions of this research and future topics are also discussed.

# II. GENERAL DESCRIPTION OF THE MAPHAM CONVERTER

## A. INTRODUCTION

In this chapter, the background of resonant converters and, more specifically, the characteristics of the Mapham converter are reviewed in detail. In addition, the entire Mapham converter circuit is scrutinized, analyzing the current conduction, the gating pulses, and of premium importance, the resonant frequency. The series connection of two resonant converters is discussed in a subsequent chapter.

## B. BACKGROUND OF RESONANT CONVERTERS

Dr. Mapham conducted the majority of his research on the Mapham parallel output resonant converter in the late 1960s which is concurrent with the time when the term *power electronics* was coined. Switching power converters were investigated and applied, however, long before the discovery and development of semiconductors. Switching power converters were first analyzed in the early 1920s, and in the late 1960s, researchers like Dr. Mapham began making significant progress in the field of power conversion, with key improvements in the area of resonant converters.

Prior to the introduction of resonant converters, pulse width modulation (PWM) was the primary means of phase and/or frequency power conversion. The purpose of PWM is to control both the output voltage amplitude and, in some cases, the size of one or more of the output's harmonic components. Variation of the pulse, width and

5

frequency, will, in turn, vary the amplitude and smoothness of the output waveform. Although practical and useful, pulse width modulation has some significant drawbacks. The most significant is high switching losses. At high frequencies, switching losses reduce the efficiency to unacceptable levels. With resonant converters, the attendant switching losses are very low at very high frequencies.

Resonant power conversion technology offers many other advantages in comparison with the PWM alternative. Among them are low electromagnetic interference, small volume and weight of components due to the high operating frequency, high efficiency, and low reverse-recovery losses in diodes because of low *di/dt* at turn-off. [Ref. 2] The SCR is the key element of the resonant converter. The SCR is gated on with a minimum gate current and it remains on until the anode-to-cathode current falls below the holding current. With the SCR, switching frequencies in the upper kilohertz are being contemplated to reduce the size and the weight of transformers and filter components and, hence, to reduce the cost as well as the size and the weight of power electronic converters.

## C. MAPHAM CONVERTER CIRCUIT

For the purposes of this thesis, the center-tapped supply configuration and the bridge configuration of the Mapham converter are analyzed and simulated. Figure 2.1 shows the center-tapped configuration in its most elementary form. The operation of the circuit is as follows: When SCR1 is triggered, current flows from the supply E1 charging up the capacitor C to a voltage approaching 2E1. As a result of the L-C

resonant tank, the current then reverses and flows back to the supply via diode D1 and C discharges. During the reverse current flow, turn-off time is presented to SCR1. SCR2 is triggered next and a similar cycle occurs in the lower half of the circuit with a negative-going voltage appearing across C. SCR1 is now triggered again and so the cycle repeats. The frequency of the output voltage waveform is thus set by the switching pulses applied to the SCRs. The values of L and C are selected so that the resonant frequency is higher than the output frequency.

The SCRs are triggered by applying a current to the gate of the thyristor. This current may be created by a pulse generator in series with a resistor. The required width of the pulse depends on the output frequency specified by the circuit designer. The resonant frequency ($f_r$) is determined by the following equation:

$$f_r = \frac{\omega_r}{2\pi}; \quad \omega_r = \frac{1}{\sqrt{LC}} \tag{2.1}$$

## D. CHARACTERISTICS OF THE MAPHAM CONVERTER

The Mapham converter is a parallel output resonant-switch dc-to-ac converter. The output voltage and waveform is affected by changes in the triggering frequency ($f_o$), the switch from an inductive to capacitive load, and changes in the ratio of $f_r/f_o$ and $L_2/L$, which are defined in Chapter III. However, the output voltage, output waveform, and peak SCR voltage remains relatively unaffected by changes in the load resistance. Figure 2.2 and Figure 2.3 show the circuit waveforms under no-load and full-load

7

conditions, respectively. Close review shows a virtually unchanged voltage output, an advantageous characteristic of the Mapham and resonant converters, in general.

Under capacitive load situations, the current through the resonant inductor leads the fundamental component of the voltage. Operation in this range is not recommended because the diodes turn off at high *di/dt*, necessitating large reverse-recovery current spikes. [Ref. 3] Figure 2.4 shows the effect of a heavy capacitive load on the circuit waveform. Note the broadening of the current pulses and the increase in output voltage. When the inductor current lags behind the fundamental component of the voltage, the diodes turn off at low *di/dt* and do not generate reverse-recovery current spikes. Figure 2.5 shows the effect of a heavy inductive load with an opposite trend. Neither leading nor lagging power factor loads experience any serious adverse effects powered by this circuit.

Figure 2.6 illustrates the effect of varying the triggering frequency ($f_o$) on the output voltage waveform while keeping the resonant frequency of the L-C circuit constant. Note that distortion of the output waveform is minimized at a ratio of $f_r/f_o = 1.35$.

## E. MAPHAM BRIDGE CONFIGURATION

The bridge configuration of the Mapham converter is shown in Figure 2.7. The operation of the circuit is as follows: SCR1 and SCR4 are triggered simultaneously and current flows through the pair charging up the capacitor C. The current then reverses direction and returns to the supply through the flyback diodes, D1 and D4, thus discharging the capacitor. By having the current resonate back through the diode,

adequate turn-off time is presented to SCR1 and SCR4 thyristor pair. While the current is returning through the flyback diodes, D1 and D4, SCR2 and SCR3 are gated on. This action accelerates the decay of the SCR1 and SCR4 current and initiates the charging of the capacitor C in the reverse direction. The current through SCR2 and SCR3 will eventually reverse, turning off the SCR1 and SCR4 and discharging C. The return current flows through the flyback diodes, D2 and D3. SCR1 and SCR4 are gated on during this return flow and the cycle repeats. Ideally then, the bridge converter operates without switching losses by switching the thyristors on zero current crossings. [Ref. 4]

In comparison with the center-tapped supply, the Mapham bridge configuration has higher output power, while the frequency range and the efficiency is relatively unaffected. The increase in output power is attributed to the increased value of the source and the longer period of SCR current conduction. The significant drawback to this circuit is the additional weight and cost of the components. The advantage is that a center-tapped supply is not required.

## F. CONCLUSION

At this point, some of the advantages and disadvantages of the Mapham converter have been identified. Advantages include near-zero switching losses, insensitivity to changes in the resistive load, and the output frequency is limited only by the switching speed of the available SCRs. Disadvantages include a slight sensitivity to capacitive/inductive loads and the need to series-tie the converters to achieve voltage control. The next step is to clarify how the converter is analyzed and designed for both

control. The next step is to clarify how the converter is analyzed and designed for both laboratory testing and PSpice simulation. It is noted that, to date, there is tremendous room for continued research by power system engineers into series connecting the Mapham bridge configuration in order to dynamically control the output voltage.
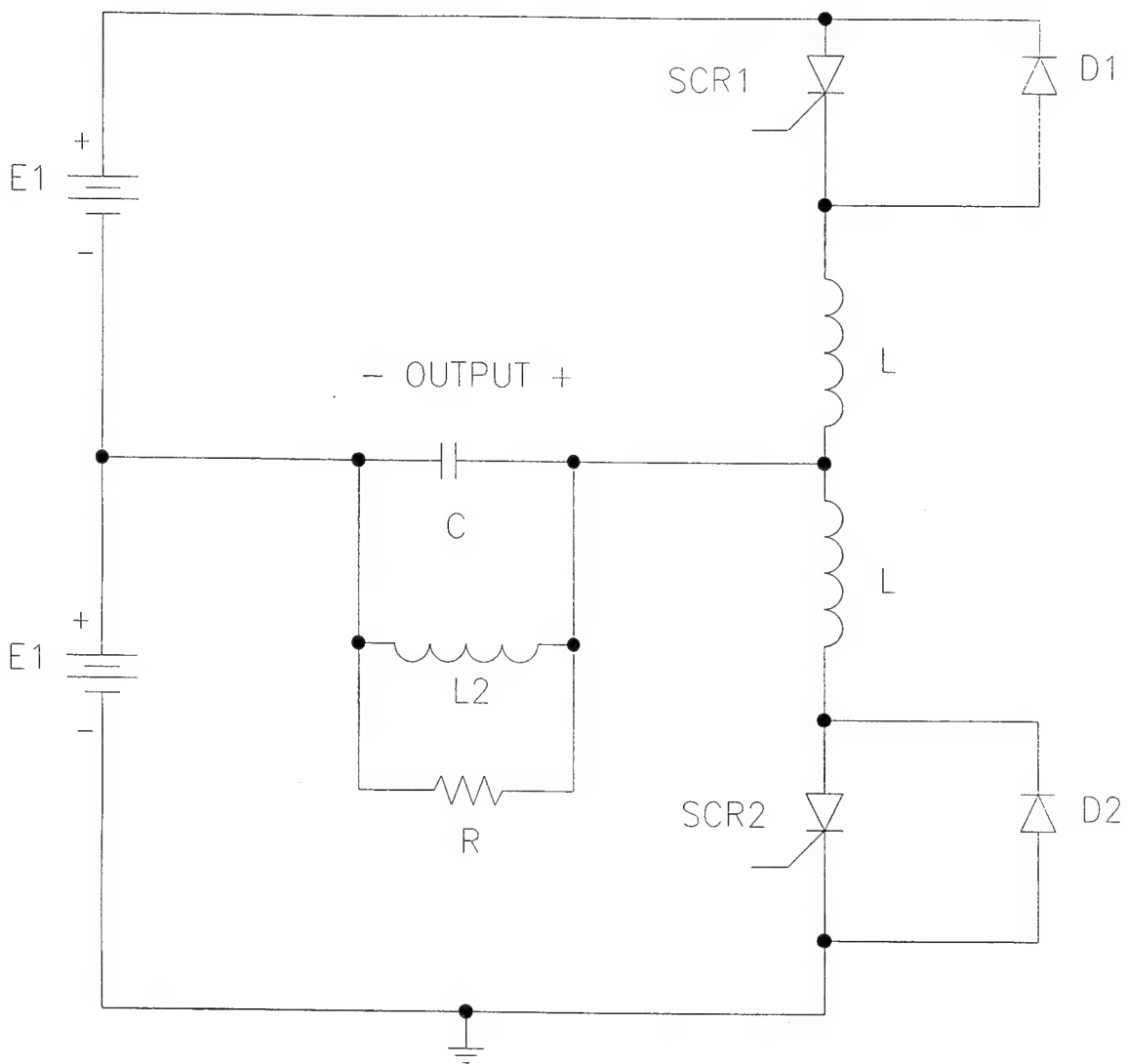
Figure 2.1  Elementary Form Of Center-Tapped Supply Mapham Converter [Ref. 1]
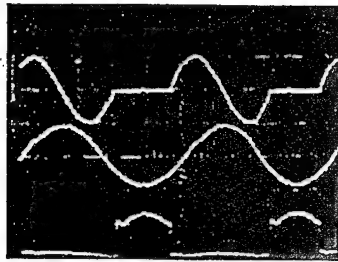
Figure 2.2 Circuit at no-load.
[Ref. 1]
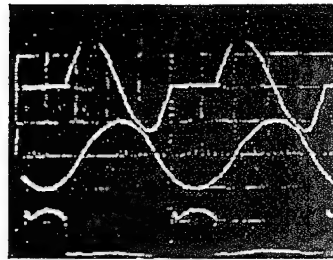


Figure 2.4 Circuit at full-load (capacitive)
[Ref. 1]
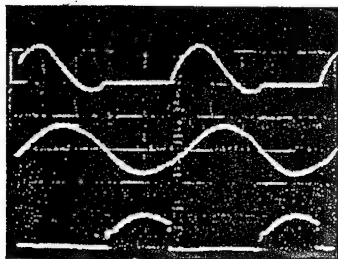


Figure 2.3 Circuit at full-load.
[Ref. 1]
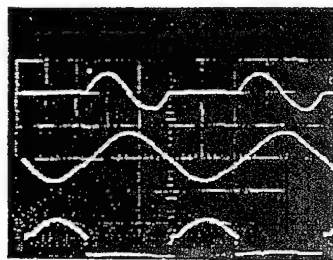


Figure 2.5 Circuit at full-load (inductive).
[Ref. 1]

Top Trace:      SCR and diode current (Is and Id)
Middle Trace:  Capacitor and Output Voltage (Vc)
Bottom Trace: SCR voltage (Vc)

12
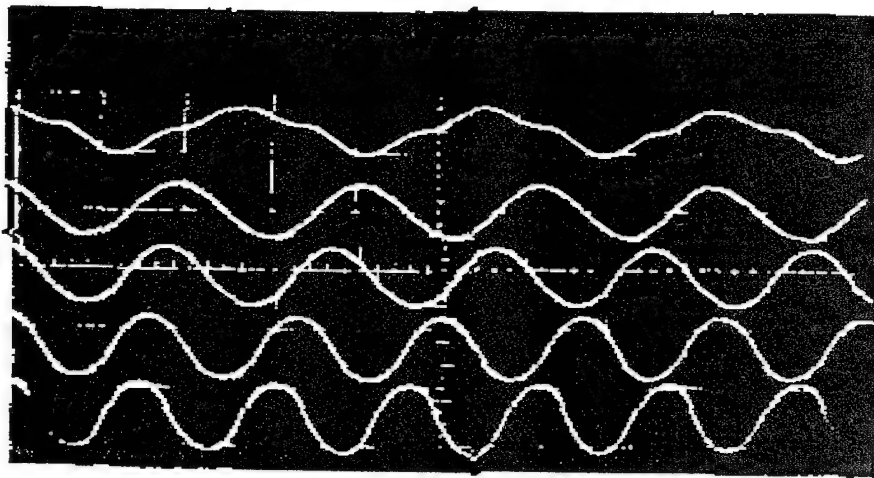
Figure 2.6    Output voltage waveforms for different ratios of resonant to triggering
frequency $(f_r/f_o)$; reading from top:  2, 1.5, 1.35, 1.2, and 1.1. [Ref. 1]

13
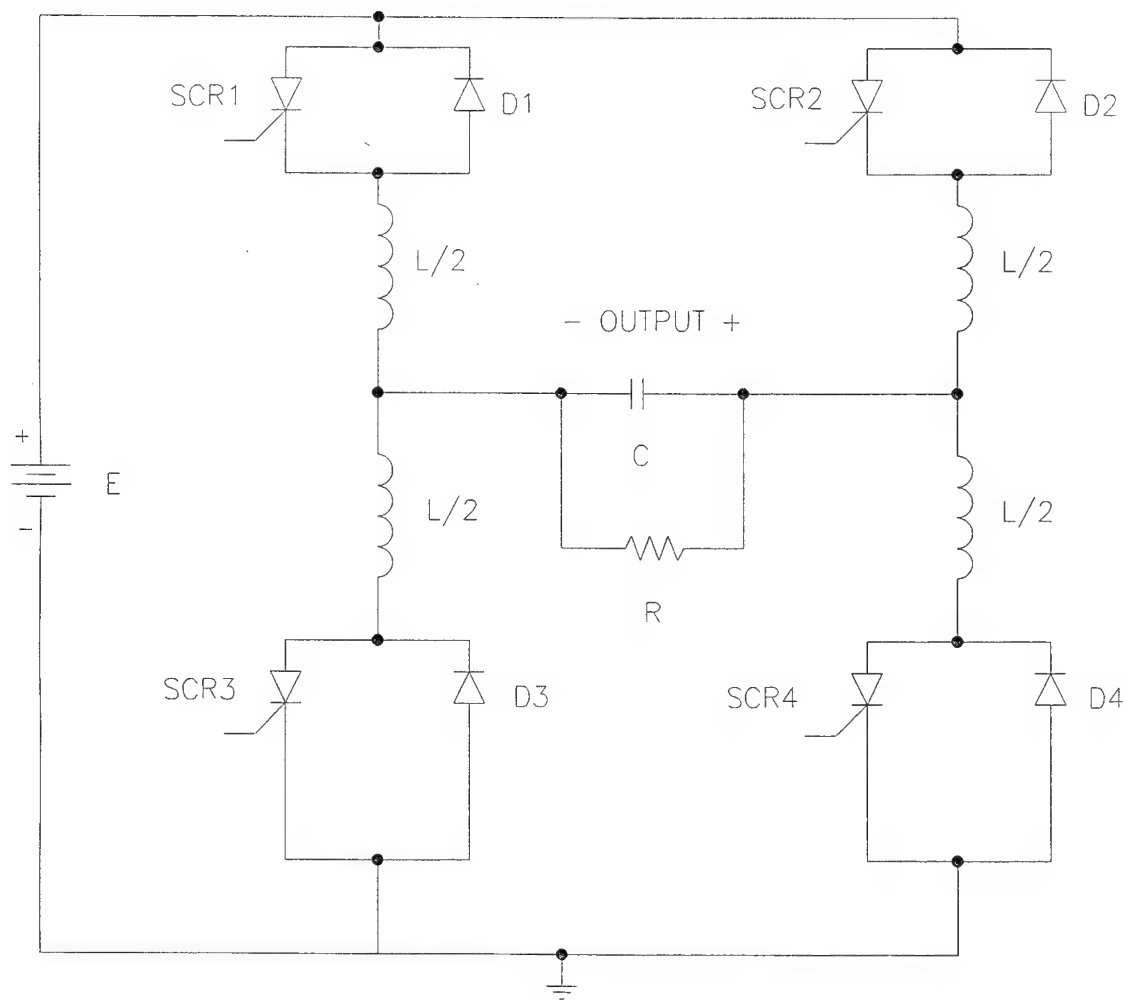
Figure 2.7    Mapham Bridge Configuration

14

# III. COMPONENT SELECTION

## A. INTRODUCTION

In this chapter, the circuit analysis, circuit configuration, and design specifications of the parallel output resonant converter are discussed. In addition, the complete design procedure is detailed step by step. Included in this design description is the criterion for selecting the SCR and diode, which are the key components in a Mapham converter circuit.

## B. GENERAL SPECIFICATIONS

In identifying the general specifications for determining the parameters, resonant frequency, and operation of the Mapham resonant converter, a thorough discussion of the circuit analysis and design specifications is detailed below. [Ref. 1, p. 177-179]

### CIRCUIT ANALYSIS

The analysis of the Mapham circuit, both the center-tapped supply and the bridge configuration, is based on the following assumptions:

1. That capacitors and inductors are pure and lossless (no series resistance);
2. That SCR's and diodes turn on instantaneously, have zero voltage drop and that there is no flow of reverse recovery current; and
3. That the power supply has zero impedance at all frequencies.

The circuit, Figure 3.1, was analyzed by numerically solving the following four differential equations.

$$E - V = L\frac{dI_1}{dt} \tag{3.1}$$

$$E + V = L\frac{dI_2}{dt} \tag{3.2}$$

$$\frac{dV}{dt} = \frac{I_1 - I_2 - I_3 - V/R}{C} \tag{3.3}$$

$$V = L_2\frac{dI_3}{dt} \tag{3.4}$$

where E is the dc source voltage, $I_1$ is the current through the upper L inductor, $I_2$ is the current through the lower L inductor, $I_3$ is the current through the load inductance L2, and V is the voltage across the output.

The opening and closing of the switches representing the SCR's and diodes were controlled by zero-current crossings. Each case was examined for as many cycles as was necessary to make the difference between succeeding peak positive and negative voltages (V) less than 0.1% (till steady-state was achieved). The solution is presented as a set of variables converted to normalized or dimensionless form by:

1. relating the load resistance R to the circuit impedance $\sqrt{L/C}$,
2. relating all voltages to the supply voltage E,
3. relating all currents to the supply voltage divided by the circuit impedance $E/\sqrt{L/C}$,
4. relating all times to the half period of the L-C circuit, $\pi\sqrt{LC}$,
5. relating the resonant frequency of the L-C circuit ($f_r$) to the output frequency or triggering frequency of one SCR ($f_o$),
6. relating the inductor $L_2$ to L.

The use of the normalized parameters enables the design data to be presented as a set of universally applicable tables with three variables: $R / \sqrt{L / C}$, $f_r/f_o$, and $L_2/L$. The Mapham Converter Design Data table is given in Appendix A.

The following definitions are applicable when using the table:

| | |
|---|---|
| $I_S$ | Peak steady-state SCR current |
| $I_D$ | Peak steady-state diode current |
| $I_{DC}$ | Average steady-state supply current |
| $V_C$ | Peak steady-state capacitor and load voltage |
| $Vc_{rms}$ | RMS steady-state, capacitor and load voltage |
| $V_S$ | Worst-case peak SCR forward and diode reverse voltage at the given value of $R / \sqrt{L / C}$ |
| $t_S$ | Pulse width of steady-state SCR current |
| $t_D$ | Pulse width of steady-state diode current and steady-state turn-off time as seen by SCR |
| $t_{min}$ | Worst-case turn-off time presented to the SCR |

## DESIGN SPECIFICATIONS

In designing power converters and inverters, the designer must already have requisite knowledge concerning:

1. The desired output power ($P_o$);
2. The desired output frequency ($f_o$);
3. The desired output waveform;
4. Load characteristics including starting loads, phase angle, duty cycle, and desired regulation;
5. The voltage (E) of the power supply to be processed and the desired output voltage.

Although outside the scope of this thesis, the following checklist of the information needed to complete the design of power processing equipment is found useful.

6. Supply voltage variations;
7. Power supply voltage transients;

17

8. Power supply short-circuit current (in order to design the protective circuitry);
9. Frequency stability;
10. The desired efficiency;
11. The need if any to make the inverter current limiting;
12. Radio frequency interference requirements;
13. Cooling fluid type and maximum and minimum temperatures;
14. Maximum weight of equipment;
15. Maximum size;
16. Any special environmental requirements;
17. Quantities;
18. Cost objectives.

## C. DESIGN PROCEDURE

The design of the Mapham converter for the specifications listed above is accomplished in the following ten steps:

1. Choose $f_r/f_o$: Figure 2.6 shows resistive-load waveforms for five values of $f_r/f_o$; select the desired resonant frequency bearing in mind that the lower values of $f_r/f_o$ give shorter turn-off times and higher device voltages.

2. Choose $L_2/L$: As most practical applications of this type of circuit need an output transformer either for isolation or voltage transformation, this analysis assumes an inductance ($L_2$), simulating the primary inductance of a transformer, across the load. Low relative values of $L_2$ drastically shorten the SCRs turn off time during starting but otherwise do not have a very significant effect on the operation of the circuit. The case of an $L_2/L$ ratio of 20 is provided in Appendix A.

3. Choose full-load $R / \sqrt{L / C}$: Low values of full-load $R / \sqrt{L / C}$ will economize in circulating current and hence in the cost of semiconductors,

18

capacitors and inductors, but at the expense of SCR turn-off time, load regulation performance and overall efficiency. A reasonable compromise is achieved by making the full-load value of $R / \sqrt{L / C}$ between 3 and 5.

4. Find $I_{DC}$: As the power output, $P_o$, and supply voltage, E, are given, the average current from the supply, $I_{DC}$, can be found by assuming, as Dr. Mapham [Ref. 1] did, that the overall efficiency, ( $\eta$ ), of the inverter will be 90%. This value can be modified if component values and costs indicate that a rerun is needed.

$$I_{DC} = \frac{P_o}{\eta E} \tag{3.5}$$

Care must be taken to choose the right value of $I_{DC}$ and E for the circuit configuration used. Failure to do so will result in damage to components because of excessive current flow.

5. Find $\sqrt{L / C}$: Having chosen $f_r/f_o$, $L_2/L$ and $R / \sqrt{L / C}$, the value of

$$I_{DC} \sqrt{L / C} / E \text{ may be read off from the table in}$$

Appendix A. As $I_{DC}$ and E are known, $\sqrt{L / C}$ can be found.

6. Voltage and current relations: Knowing $\sqrt{L / C}$ and E, the following can be found by multiplying the table values of current and voltage ratios by

$E / \sqrt{L / C}$ and E, respectively: $I_S$, $I_D$, $V_C$, and $VC_{rms}$.

19

7. Find $\pi\sqrt{LC}$: Knowing the desired output frequency, $f_o$, the half period of the L-C circuit may be found from:

$$\pi LC = \frac{10^6}{(2)(f_r)(f_o)} \quad \mu s \quad (\mu H, \mu F \text{ and Hz units}) \tag{3.6}$$

8. Time relations: As $\pi\sqrt{LC}$ is known, find $t_S$, $t_D$ and $t_{min}$ by multiplying the table value in Appendix A by $\pi\sqrt{LC}$.

9. Resonant frequency: With $f_r/f_o$ selected in step 1 and $f_o$ given, the resonant frequency is calculated from:

$$f_r = \frac{f_r}{f_o} \times f_o \quad Hz$$

10. Component values: Knowing $\sqrt{L/C}$ and $f_r$, R, L, $L_2$ and C may be found.

$$R = \frac{R}{\sqrt{L/C}}\sqrt{L/C} \quad \Omega \text{ ohms} \tag{3.7}$$

$$L = \frac{\sqrt{L/C}}{(2\pi f_r)}10^6 \quad \mu H \tag{3.8}$$

$$C = \frac{10^6}{2\pi f_r \sqrt{L/C}} \quad \mu F \tag{3.9}$$

## D. CHOOSING THE SCR AND DIODE

The SCR and diode are specified as follows:

Issues that must be considered in choosing the SCR include:

1. The peak forward voltage $= V_S$
2. The peak current $= I_S$
3. The repetition rate of the current pulse $= f_o$
4. The pulse width of the current $= t_S$
5. The minimum turn-off time presented to the SCR $= t_{min}$

The only parameter which is unknown is the rate of change of the anode-to-cathode voltage (*dv/dt*). The *dv/dt* depends on the value of the series R-C snubber circuit in parallel with the SCR which damps out the ringing due to circuit inductance. The inductor should have as little distributed capacitance as possible in order to keep the losses in the damping R-C circuit low.

Issues that must be considered in choosing the diode include:

1. The peak reverse voltage = $V_S$ = peak forward SCR voltage

2. The pulse width of current = $t_D$

3. The repetition rate of the current pulse = $f_o$

As evidenced from a review of Figures 2.5 and 2.6, current peaks are greater under lightly loaded conditions. Therefore, the diode current is highest when the circuit is lightly loaded, and hence the diode current $I_D$ should be calculated using the highest value of $R / \sqrt{L / C}$ liable to be encountered in practice.

## E. LABORATORY DESIGN OF MAPHAM CONVERTER

The design process for the center-tapped supply Mapham configuration built in the Power Systems Laboratory is provided below:

1. Choose $f_r/f_o$: For minimal distortion, the researcher selected $f_r/f_o$ to equal 1.35. An output frequency, $f_o$, of 60 Hz was selected because the thyristor circuitry in the laboratory was designed for operation in the 50-60 Hertz frequency range. Further explanation is provided in Chapter V.

21

2. Choose $L_2/L$: The researcher selected $L_2/L$ to equal 20. This parameter was selected because it best corresponded with the turn-off time of the thyristors used in the laboratory.

3. Choose $R / \sqrt{L / C}$: The researcher selected $R / \sqrt{L / C}$ to equal 5.

4. Find $I_{DC}$: With a selected $P_o$ of 250 Watts, an input voltage $E = 75$ Volts, and an assumed efficiency of 90% :

$$I_{DC} = \frac{250 \text{ Watts}}{(0.9)(150 \text{ V})} = 1.85 \text{ Amps average}$$

5. Find $\sqrt{L / C}$: With $f_r / f_o$, $L_2 / L$ and $R / \sqrt{L / C}$ chosen, the Table 2 of Appendix A reads that $\sqrt{L / C} / E$ is 0.229.

6. Voltage and current relations:

$$I_S = 11.88 \text{ Amperes (peak)}$$

$$I_D = 5.65 \text{ Amperes (peak)}$$

$$V_C = 160.5 \text{ Volts (peak)}$$

$$V_{crms} = 113 \text{ Volts (peak)}$$

7. Find $\pi\sqrt{LC}$: Knowing the desired output frequency, $f_o$, the half period of the L-C circuit may be found from:

$$\pi LC = \frac{10^6}{(1.35)(60\text{Hz})(2)} = 6172.8\mu s$$

8. Time relations:

$$t_S = 6.17 \text{ ms}$$

$$t_D = 4.136 \text{ ms}$$

$$t_{min} = 2.16 \text{ ms}$$

9. Resonant frequency:

$$f_r = (1.35)(60\text{Hz}) = 81 \text{ Hz}$$

10. Component values: Knowing $\sqrt{L / C}$ and $f_r$:

$$R = 46.4 \ \Omega$$

$$L = 6.63 \ \text{mH}$$

$$C = 544 \ \mu\text{F}$$

## RESULTS OF LABORATORY DESIGN

From the design parameters specified and detailed above, the center-tapped

supply Mapham converter was constructed and tested in the Power Systems Laboratory

and the following theoretical versus actual data was tabulated in Table 3.1. The

parameters, $f_o$, $f_r$, R, L, and C, theoretical values were obtained from design and the

actual values were obtained from oscilloscope, inductance meter, and laboratory

measurements.

23

Center-Tapped Supply Mapham Converter Laboratory Data

| Parameter | Theoretical Values | Experimental Values |
|-----------|--------------------|--------------------|
| $f_o$ | 60 Hz | 60 Hz |
| $f_r$ | 81 Hz | 86.5 Hz |
| R | 46.4 $\Omega$ | 45.15 $\Omega$ |
| L | 6.63 mH | 6.75 mH |
| $L_2$ | 132.6 mH | 127.5 mH |
| C | 544 $\mu F$ | 570 $\mu F$ |

Table 3.1

## F. CONCLUSION

The center-tapped supply Mapham configuration design procedure, including

specifics for the key elements, the SCR and diode, has been detailed. Table 3.1 shows

the differences between the theoretical design and the actual values used in the

laboratory. In the next chapter, a detailed look at the PSpice simulation process is

provided. A comparative breakdown of the differences between PSpice and laboratory
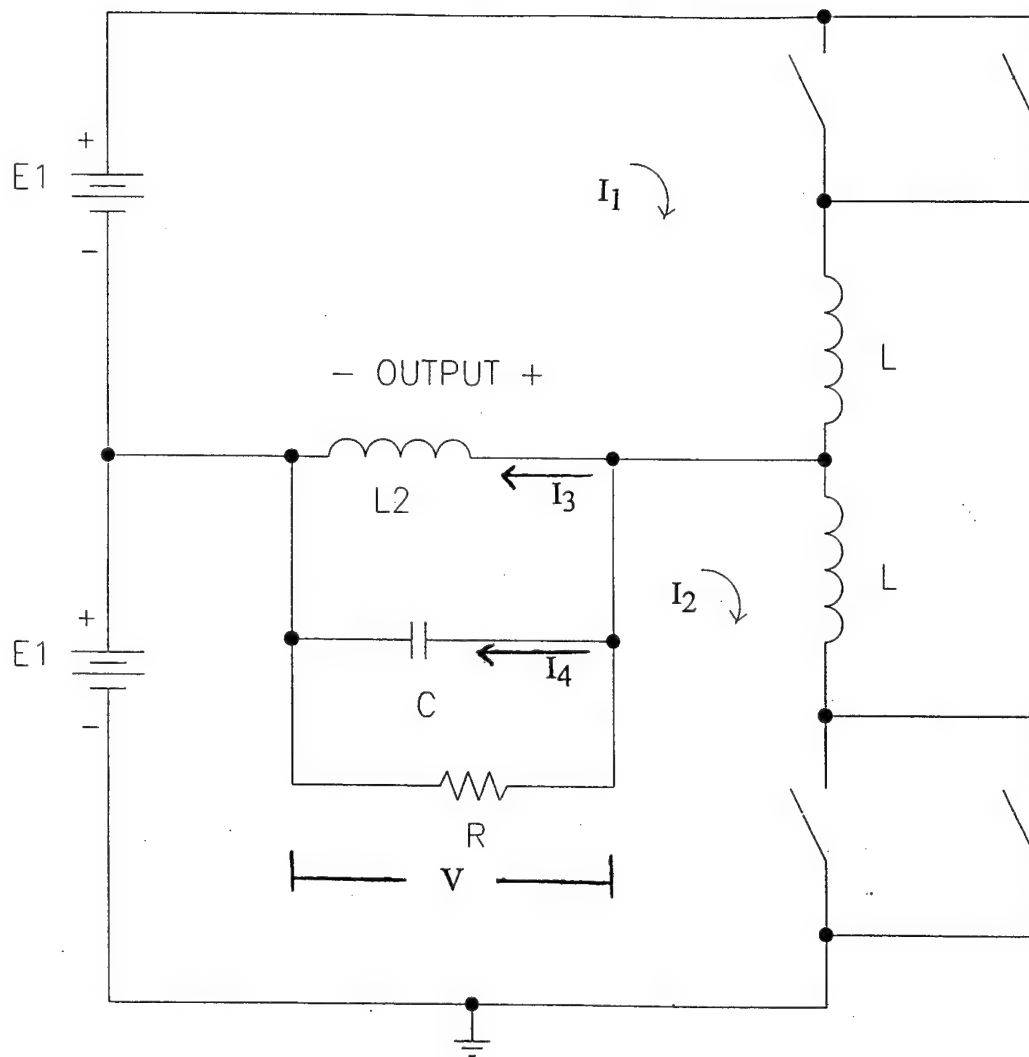
testing is given, as well.

Figure 3.1    Center-Tapped Circuit Information For Computer Simulation [Ref. 1]

25

# IV. PSPICE SIMULATION

## A. INTRODUCTION

An important supplement to the laboratory analysis of the Mapham converter is an accurate PSpice simulation. In this chapter, an overview of the PSpice software, its various capabilities and limitations, the gate drives, and other key information are delineated.

## B. OVERVIEW OF PSPICE

SPICE, from the University of California, at Berkeley, is the *de facto* world standard for analog circuit simulation. PSpice, from MicroSim Corporation, is one of the many commercial derivatives of U.C. Berkeley SPICE. PSpice was the first SPICE-derived circuit simulator available on the IBM personal computer, and was later introduced on the SUN network. PSpice is seven years old, with over 14,000 professional copies in use.

PSpice allows the designer to simulate an electrical circuit design before the circuit is built, which, in turn, allows the designer to decide if changes are necessary, without building the hardware. PSpice also helps to check the design after it is completed. This lets the designer decide if the circuit will work correctly outside the laboratory environment. In short, PSpice is a simulated "lab bench" on which test circuits and measurements are made. However, PSpice will not design the circuit.

27

The practical way to check an electrical circuit design is to build it. However, by the early 1970s, the components that were contained on an integrated circuit had become much smaller than individual discrete components. Physical effects that were negligible for normal circuits, such as a stereo amplifier, became important for these microcircuits. So the circuits could not be assembled from components in the lab and give the correct test results; the circuit had to be either (i) physically built, which expensive and time consuming, or (ii) carefully simulated using a computer program. This is why the acronym SPICE stands for Simulation Program with Integrated Circuit Emphasis. [Ref. 5]

In the case of the center-tapped supply configuration, Figure 3.1, the evaluation 6.2 version of Pspice was utilized and the simulation results appeared as expected. Only slight modifications were required for effective simulation. These modifications are discussed in detail in Chapter V. The evaluation 6.2 version, however, was limited in node capacity (64 to be exact), and as a result of this limitation, the professional 5.3 version was utilized to simulate the bridge configuration.

The evaluation 6.2 version and the professional 5.3 version are very similar in operational architecture. To better understand PSpice's architecture, a discussion of the circuit file set, the model library, the simulation output file, the probe data file, the probe, and the simulation setup are reviewed. Figure 4.1 illustrates a general block diagram of PSpice operational architecture.

28

CIRCUIT FILE SET

Initially, the designer must build the circuit using the schematic capture capability of the software. After the circuit has been constructed and saved with a filename, "the simulator must be supplied with a *netlist* description of the circuit to be simulated. Figure 4.2 provides an example of a netlist and simulation setup within a circuit file. In addition, the simulator must be supplied with the *simulation directives* specifying which analyses are to be performed and stating any relevant simulation controls. This information is provided in the circuit file set, which is the primary source of input to the simulator.

The circuit file set is made up of the following files:

- The primary *circuit file* (<*schematic name*>.cir) containing analysis commands, simulation control commands, and references to the netlist, alias, model, and other files required by the circuit to be simulated.

- The *netlist file* (<*schematic name*>.net) which describes the components and connections of the circuit in standard netlist format.

- The *alias file* (<*schematic name*>.als) which provides a mapping between the Schematics part and pin names and the simulator device and node names.

The generation of the circuit file set is automatic through the Schematics interface using the Analysis/Create Netlist command. [Ref. 6, p. 14]

## THE MODEL LIBRARY

Every MicroSim product installation is shipped with a Model Library containing the electrical definition of an extensive array of common analog and digital devices. Each definition corresponds to a part symbol in the Symbol Library, and in most cases, a package definition in the Package Library. These device definitions exist in two forms: device models and subcircuits. Device models provide a means for describing a primitive part by a set of behavioral parameters. Subcircuits are functional groupings of components to which elements in external circuits can be connected.

The Model Library is comprised of a collection of individual model files. Taken together, the device definitions contained in these files are sufficient for most design requirements. However, since model files are not encrypted, and since the device definitions in these files use standard simulator command syntax, specialized models and subcircuits may be defined. This feature in PSpice was essential for the Mapham converter circuit. For accurate simulation, the thyristor provided in the Model Library was renamed and a modified new model created. [Ref. 6, p. 14-15]

## SIMULATION OUTPUT FILE

The simulation output file is an ASCII text file containing lists and tables which describe the input circuit, the analysis directives, and the results of the specified simulations; in essence, an audit trail of simulation events and results. Simulation output file content is directed by the kinds of analysis run, and options enabled in the

Analysis/Setup/Options display. Any warning or error messages encountered during read-in or simulation are also stored in this file. [Ref. 6, p. 16]

### PROBE DATA FILE

The probe data file contains simulation results to be viewed and manipulated interactively with the graphical waveform analyzer program, Probe. As the simulation proceeds, the simulator, by default, updates the Probe data file with all of the simulation results. To analyze results, the simulator can be instructed to save a subset of results by placing markers in the schematic at the nets, pins, and devices. [Ref. 6, p. 17]

### PROBE

Probe reads the data stored in the Probe data file and displays waveforms reflecting circuit response at the marked nets, pins, and devices in the schematic (via the **Markers Menu** in the Schematic Editor), or for output variables specified in Probe (via **Trace/Add** in Probe). Besides the benefit of analyzing data visually on the screen, the results can be further manipulated through expressions and search functions. Families of curves can be displayed on a single plot. In addition, Probe's messaging feature helps to pinpoint design errors; detailed message text can be displayed along with the corresponding waveforms.

Analyzing data in Probe can assist in determining the validity of the design. Both the schematic and simulation setup parameters can be refined based upon earlier results, thus creating an iterative process for running simulations and Probe analyses. [Ref. 6, p. 17]

31

SIMULATION SETUP

To run a simulation from Schematics, a number of steps must be completed. These are:

- place and connect part symbols representing the circuit to be simulated.

- set operational characteristics of the part instances by setting associated attributes, e.g., resistor value.

- enable and specify one or more analyses.

- fine tune *simulation operation* by enabling/specifying control options, if necessary.

- fine tune *output* by enabling/specifying control options, if necessary.

## C.  MAPHAM IMPLEMENTATION USING PSPICE

Certain key features were utilized for implementing the Mapham converter in PSpice.  In particular, the thyristors were gated with a 20 Volt pulse in series with a 2 ohm resistor.  These values were obtained via trial and error.  The diodes selected were 1N3883s which, by far, met the peak reverse voltage requirement.  The gate pulses, DC sources, resistor, capacitor, and inductors were simply selected from the **Get A New Part** column of the Schematic Editor.

## D.  PSPICE SIMULATION EXAMPLE

From the design provided in Section 3.5, the center-tapped source Mapham converter circuit was constructed and simulated using the PSpice 6.2 evaluation version.  Figure 4.3 and Figure 4.4 show the circuit and its simulated output.  The

32

simulation shows the inductor current and the ac output voltage. A comparison of the results in Figure 4.5 shows little difference between PSpice simulation data and laboratory data, identifying Pspice as an excellent simulation tool for the Mapham converter. With the accuracy in simulation of the center-tapped source at 60 Hz, additional simulations were conducted at 120 and 240 Hz. The results are shown in Figure 4.6 and Figure 4.7. In addition, Figure 4.8 and Figure 4.9 show the PSpice construction and simulation of the Mapham bridge configuration at 20 kHz. Parameter values are specified in Table 4.1 and were obtained using the same procedure for the center-tapped supply.

Mapham Bridge Configuration Parameters

| R = 12.5 Ω | L = 30μH | C = 4.7μF | $f_o$ = 20 kHz |
|---|---|---|---|

Table 4.1

## F. CONCLUSION

PSpice is very useful for computer simulation of the Mapham converter. Construction of both the center-tapped supply and the bridge configurations were accurately simulated using PSpice. For both configurations, various frequencies and load resistances were evaluated, exhibiting PSpice's excellent simulation capability at a wide range of frequencies and load resistances.
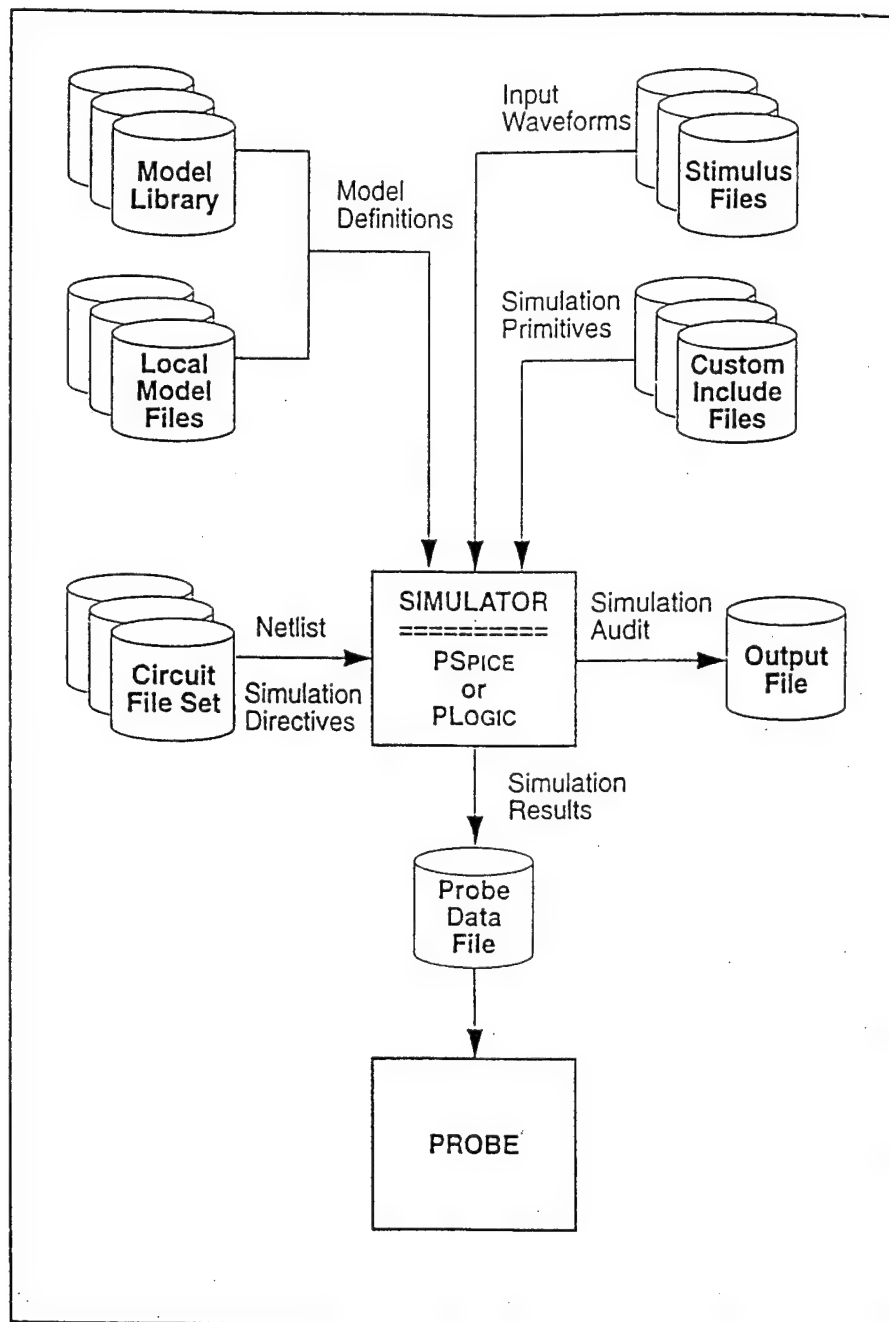
Figure 4.1    General Block Diagram of PSpice Operational Architecture [Ref. 5]

34

```
An Illustration of Circuit File Topology

* The first line in this file is the "title line"; the information typed
* after an asterisk is a "comment."  The next command defines the FACTOR
* parameter used in the netlist.
.PARAM FACTOR=1.2

* The following statements describe the circuit to PSpice.  It is a simple
* differential pair, with +12 and -12 volts as the supplies.

VIN 100 0 AC 1 SIN(0 0.1 1MEG)
VCC 101 0 DC {10*FACTOR}
VEE 102 0 {-10*FACTOR}
Q1 4 2 6 QNL
Q2 5 3 6 QNL
RS1 100 2 1K
RS2 3 0 1K
RC1 4 101 CRES 10K
RC2 5 101 CRES 10K
Q3 6 7 102 QNL
Q4 7 7 102 QNL
RBIAS 7 101 20K
CLOAD 4 5 5PF
E2 10 0 (4,5) 10
RE1 10 comp_out 200
CCOMP comp_out 0 20pf

* These commands define new models based upon the intrinsic RES and NPN
* models.  Note the use of the continuation mark "+".
.MODEL CRES RES (R=1 DEV=5% TC1=.02 TC2=.0045)
.MODEL QNL NPN (BF=80 RB=100 CCS=2PF TF=0.3NS TR=6NS CJE=3PF
+ CJC=2PF VA=50)

* The next "command line" sets the temperature for the run to
* 35 degrees celsius
.TEMP 35

* This command tells PSpice to perform a DC sweep.  The voltage source VIN
* is swept from -0.125 volts to 0.125 volts in steps of 0.005 volts.
.DC VIN -0.125 0.125 0.005

* The .PROBE command tells PSpice to write the simulation results to the
* Probe data file.  The .END indicates the end of the circuit file.
.PROBE
.END
```

Figure 4.2    Netlist And Simulation Setup Within A Circuit File [Ref. 5]
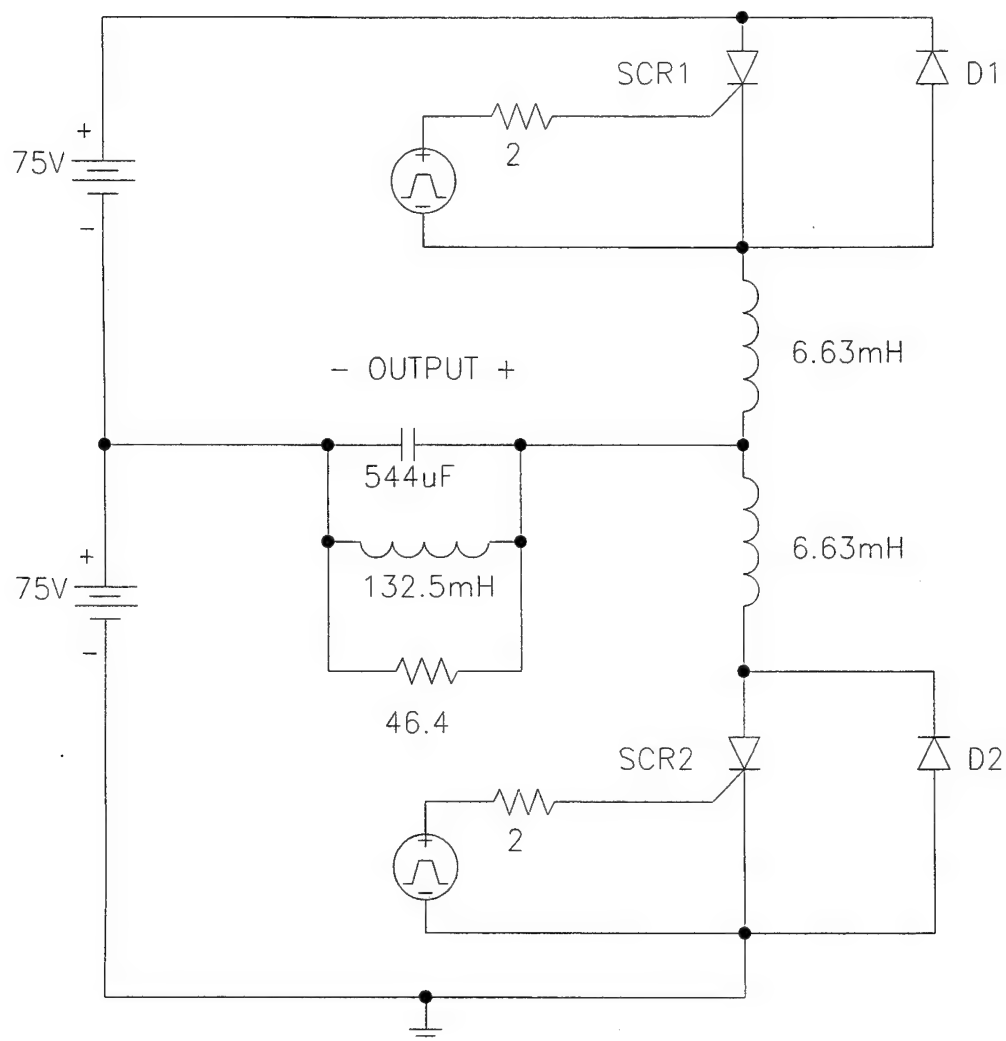
Figure 4.3    Center-Tapped Supply Mapham Converter Constructed in PSpice
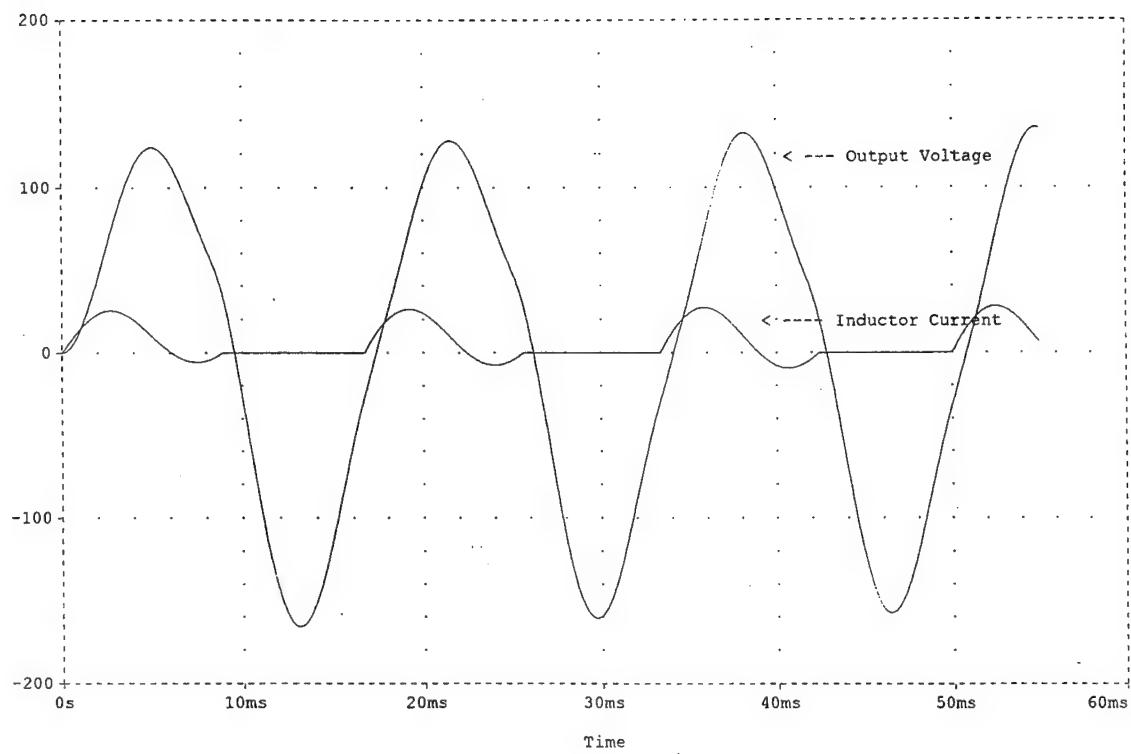
Figure 4.4    Inductor Current and Output Voltage of Center-Tapped Supply at 60 Hz

37

50V/DIV           2A/DIV           $R = 45.15\Omega$
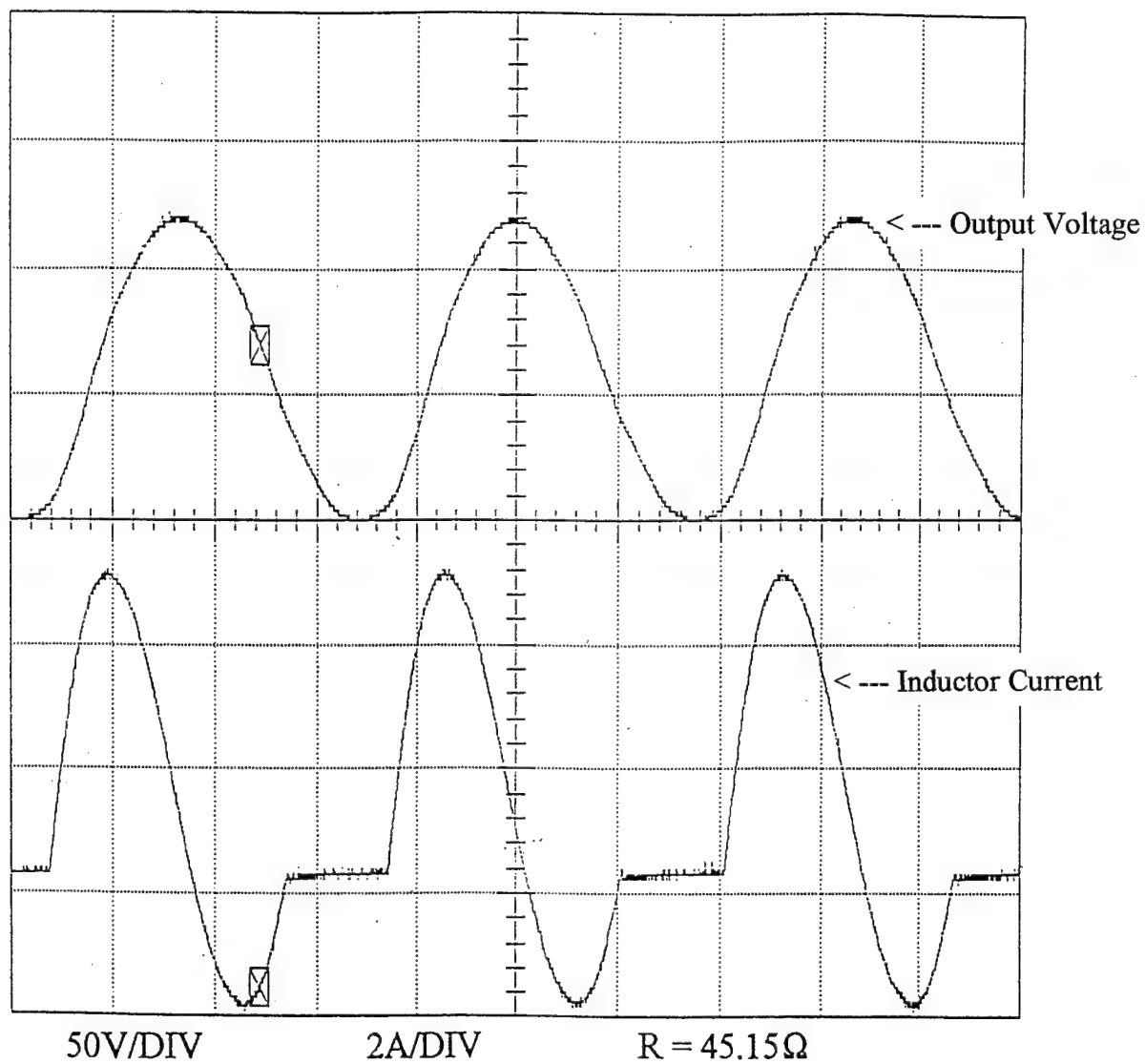
Figure 4.5    Output Waveforms of Center-Tapped Supply in the Laboratory at 60 Hz

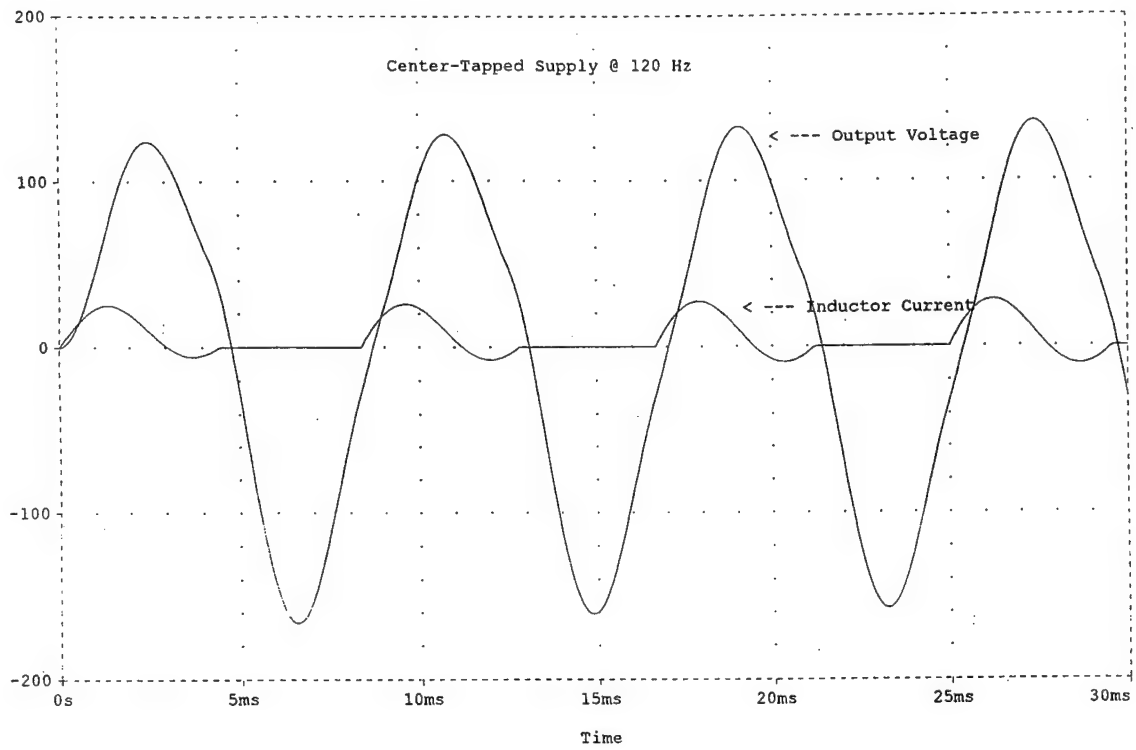Figure 4.6    Inductor Current and Output Voltage of Center-Tapped Supply at 120 Hz
(R = 46.4Ω)
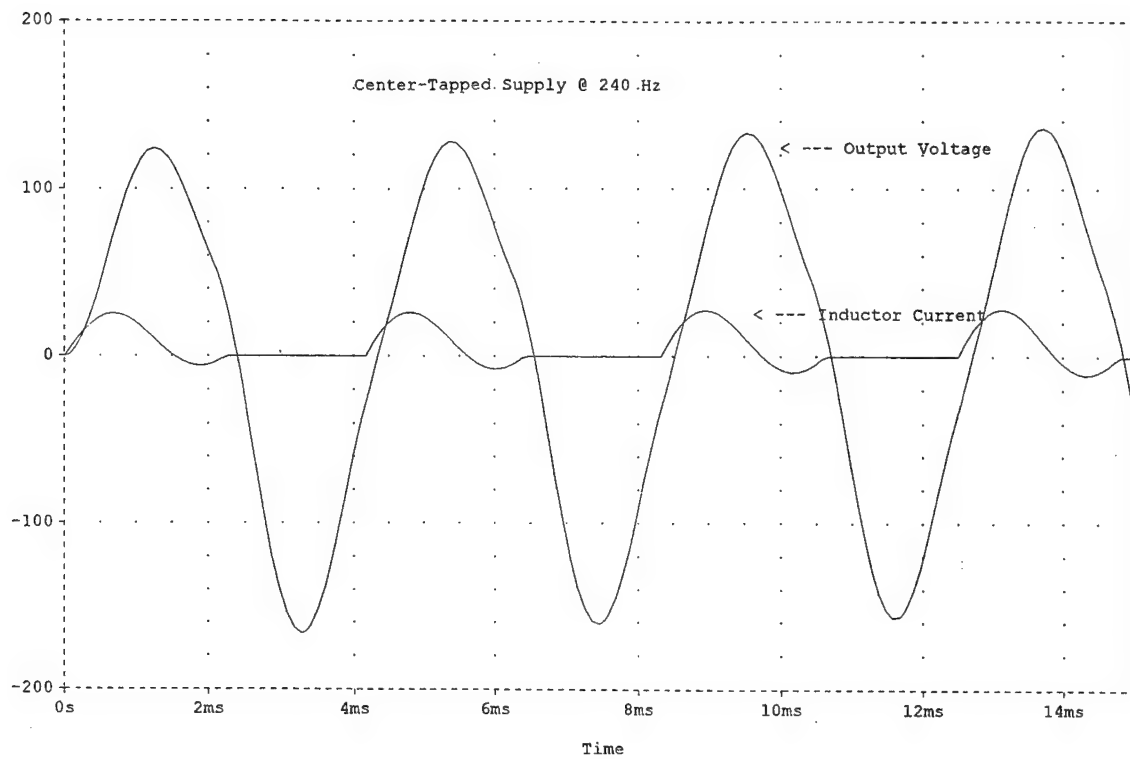
Figure 4.7    Inductor Current and Output Voltage of Center-Tapped Supply at 240 Hz
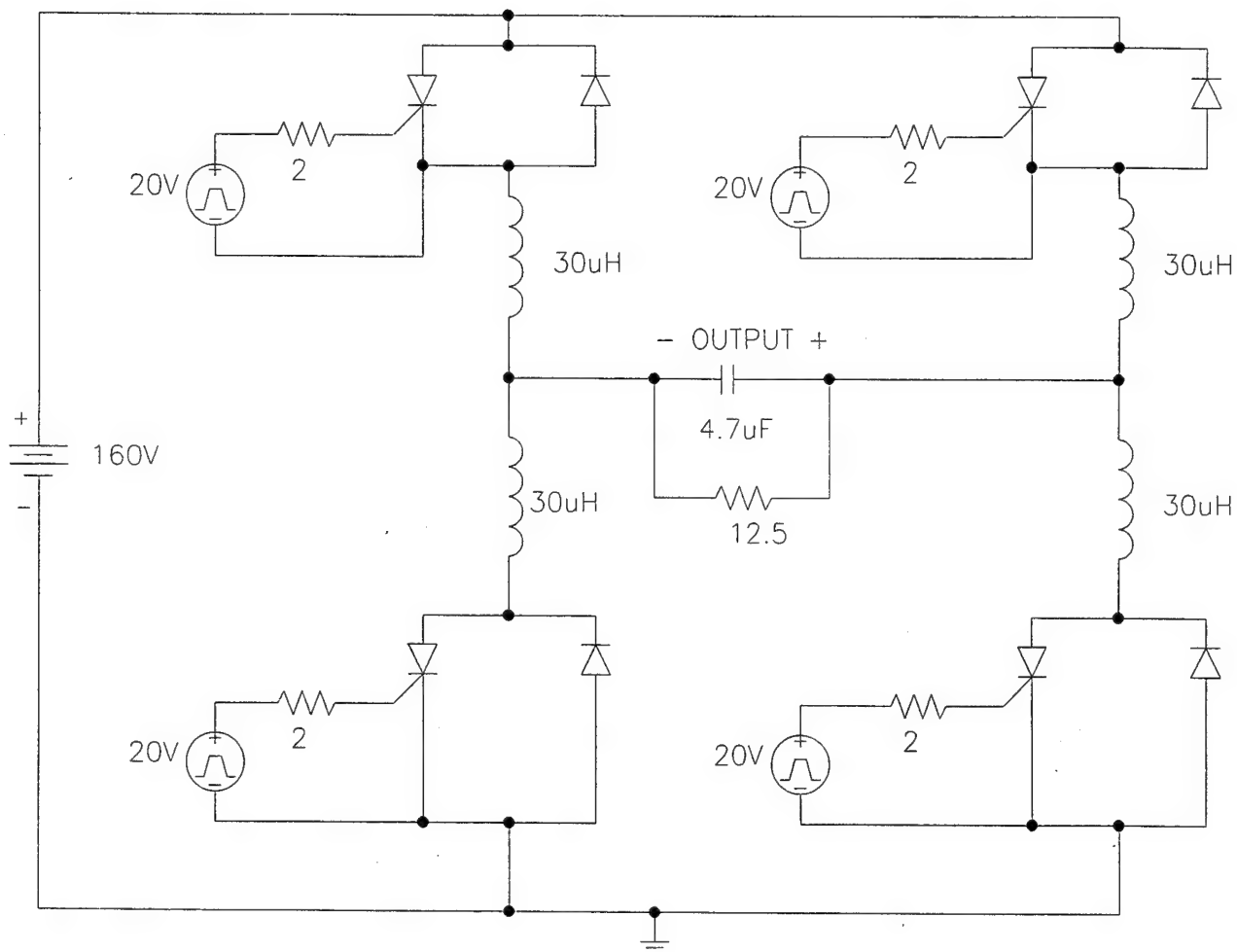             (R = 46.4Ω)

40

Figure 4.8     Mapham Bridge Converter Constructed in PSpice

41

Inductor Current and Output Voltage of Mapham Bridge @ 20 kHz
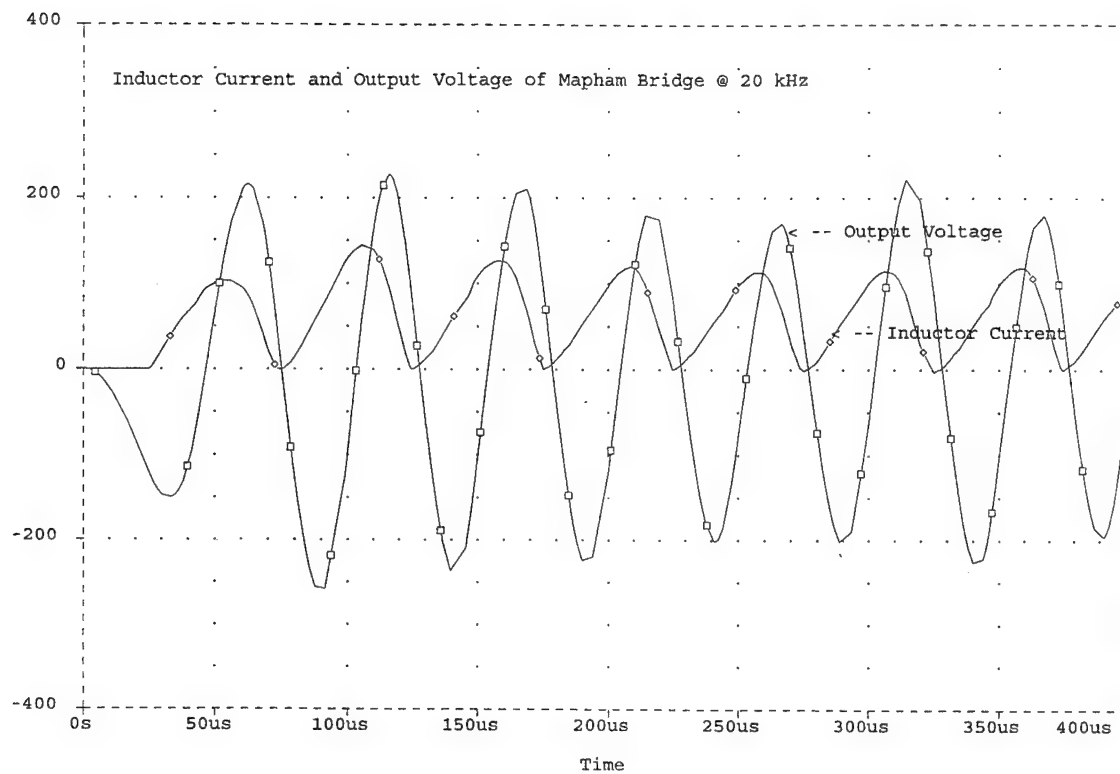
Figure 4.9      PSpice Simulation Result of Mapham Bridge Converter

# V. HARDWARE IMPLEMENTATION

## A. INTRODUCTION

In this chapter, a detailed part description and specifications for all components are given. Specifically, the thyristors, diodes, inductances, resistors, capacitors, source, pulse generators, and other components are described. Also, implementation issues from both the laboratory testing and PSpice simulation are addressed. The chapter then concludes with test studies of the center-tapped supply Mapham converter constructed in the Power Systems Laboratory. Variations in the load resistance, capacitance, and inductance are evaluated. In addition, differences in the results obtained with PSpice and in the laboratory are discussed.

## B. COMPONENT SELECTION

In the Power Systems Laboratory, the following components were required for the Mapham converter hardware design:

### VARIABLE AC/DC POWER SUPPLY

The variable ac/dc power supply was manufactured by Westcode, model no. P102-PC. Internal to the supply is the firing circuitry for the thyristor, the thyristor itself, and the snubber circuit. The 24 Volt dc voltage is provided by the Six Channel Pulse Amplifier, described later, for turn-on of the thyristors. Figure 5.1 provides a detailed description of the thyristor and the snubber component values. The power supply has a 50 Amp, 240 Volt capacity. The thyristors are N-type for application at 50 to 60 Hertz, and they have a 75 Amp, 1200 Volt capacity. From design, the anticipated

43

peak current through the thyristors was 11.88 Amps. The actual measured current reading was 11.32 Amps.

### DIODES

The diodes were manufactured by B.B.S., part no. P080PH12-FHD. They have a 35 Amp and 1600 Volt peak reverse voltage capacity. Their placement in the center-tapped supply circuit Is given in Figure 2.1. From design, the expected peak diode current was 5.65 Amps. The actual measured current was 5.66 Amps.

### INDUCTANCES

The inductors were manufactured by Arnold Engineering, part no. A254168-Z-GR. They have a maximum capacity of 42.5 mH and 10 Amp rms. Also, they are provided with incremental taps from 5 to 100 percent of maximum value. The tolerance rating is $\pm$ 10%. In the laboratory at 75 Volts, the maximum current reached was 7.56 Amps rms. At 60 Hz, six inductor modules were used, weighing between 25 to 30 pounds each. In comparison, at 1 kHz, only one module is required, showing the significant weight reduction at higher frequencies.

### RESISTORS

The resistors were manufactured by Cromalox, part no. OF1901. They have a 1 kW, 230 Volt capacity. The module is adjustable with a range varying from 23.2 $\Omega$, for full-load, to 119 $\Omega$, at light-load.

## CAPACITORS

The capacitors were manufactured by General Electric with a voltage rating and current rating of 440 Volts rms and 20 Amps rms, respectively. In the laboratory, the maximum capacitor rms voltage obtained was 151.5 Volts which is within 7% of the anticipated value. To implement the laboratory design, an assortment of capacitors were employed. In particular, capacitor values of 5 μF, 25 μF, 70 μF, and 100 μF were utilized to realize the 570 μH capacitor.

## SOURCE

To obtain the two equal dc sources needed for the center-tapped supply Mapham converter, a unique construction, identified in Figure 5.2, was required. The Variacs were manufactured by Powerstat. They provide a range of voltages from 0 to 280 Volts (RMS), and they have a power limitation of 15 kVA. The N-92MD isolation transformer is manufactured by MagneTek and it is needed to prevent a short circuit between the two sources. The transformer is designed to operate in the 50/60 Hz range with a 1 kW capacity.

## PULSE GENERATORS

The pulse function generators operate up to 20 MHz and are manufactured by WaveTek, model no. 145. The pulse generators are synchronized manually with a non-overlapping duty cycle. An overlapping duty cycle turns on both SCRs simultaneously, resulting in a fault condition.

45

## LOGIC POWER SUPPLY / SIX CHANNEL PULSE AMPLIFIER

The logic power supply, part no. L101PS, and the six channel pulse amplifier, part no. L100AM, are both manufactured by Inverpower Electronics. The logic power supply provides a 12 Volt peak-to-peak pulse to the amplifier. The amplifier is designed to magnify the pulse to 24 Volts peak-to-peak which is required for firing the center-tapped supply thyristors.

## VOLTAGE ISOLATORS

The voltage isolators were manufactured by Inverpower Electronics, L102VI. They serve to isolate a voltage so that it can be viewed on the oscilloscope, without causing a ground loop fault.

## OSCILLOSCOPE

The oscilloscope used in the laboratory was the Tektronix 2212, 60 MHz Digital Oscilloscope. It is used to view voltage and current values at various locations in the circuit.

## CURRENT PROBE AMPLIFIER

The Tektronix AM503A current probe amplifier was used to amplify or reduce the magnitude of current values. The amplifier has settings from 0.5 to 5.0 Amps/Div.

## PRINTER

The printer used was the BJ-300 Canon bubble jet printer.

46

## C. IMPLEMENTATION ISSUES

As research of the Mapham converter progressed, several implementation issues in both the laboratory and PSpice computer simulation were identified. These issues are detailed below:

### LABORATORY ISSUES

Before going into the lab, the Mapham converter was successfully simulated in PSpice at 20 kHz, which is the frequency reported in Dr. Mapham's paper. Upon considering laboratory implementation, the initial intent was to test the Mapham converter at 20 kHz. Unfortunately, this frequency was found to be impractical for two reasons: 1) the upper limit for pulse synchronization is 5 kHz and 2) the thyristors in the laboratory are designed to operate at 50/60 Hz. All efforts to synchronize the pulse generators available in the laboratory above 5 kHz were unsuccessful. Higher speed thyristors can be used for frequencies above 60 Hz, but construction of the firing circuitry with magnetic isolation is required. Also, snubber design for the thyristors must be considered. These implementation issues significantly effected laboratory testing, and as a result, the high-frequency advantages of the resonant converter, including smaller components, were not made apparent in the hardware realization.

### PSPICE ISSUES

The PSpice implementation issues are much more diversified. The initial attempts at simulation of the Mapham converter were unsuccessful. All attempts returned "transient analysis error " messages. MicroSim PSpice expert, Brian Hirasuna,

47

was contacted and a visit to Irvine, CA was made to address the problem. It was determined from trial and error that several modifications would be necessary for the circuit to simulate properly. For testing at all frequencies, the modifications include:

- the holding current for the SCR had to be set to 1 Ampere.

- in the **Options** windows, the Absolute Tolerance (ABSTOL), Iteration Limit (ITL4), and the Relative Accuracy For Voltages And Currents (RELTOL) settings had to be adjusted from their respective default values of 1 pA, 10 iterations per simulation, and 0.1% tolerance to 1 $\mu$A, 40 iterations per simulation, and 1% tolerance.

- the gate drives required a much higher current in PSpice than what is required in practice.

Each modification was rather significant. Without the change in the holding current, the SCRs would not have sensed a low enough holding current, preventing the SCR from properly turning on and turning off. The ABSTOL , ITL4, and RELTOL were all increased to compensate for the higher voltages and currents of the Mapham converter as opposed to an integrated circuit. The adjustments enabled Pspice to conduct transient analysis. The RELTOL was found to be the most critical element of the three options.

**D. HARDWARE TEST STUDIES**

Figure 4.5 is the oscilloscope waveform of output voltage and inductor current of the center-tapped supply Mapham converter constructed with design specifications,

described in Section 3.5, for 60 Hz and a resistive load of 45.15 $\Omega$. At this same

frequency, test studies were conducted on this circuit in the Power Systems Laboratory.

The load resistance was increased from 45.15 $\Omega$ to 23.2 $\Omega$. Capacitance was increased

from 500 to 700 $\mu$F, and inductance was increased from 6.75 to 12.75 mH. In the case

of load resistance variation, Figure 5.3 shows an advantageous feature of the converter.

In comparison with Figure 4.5, the output voltage waveform is virtually unchanged.

Also, the inductor current waveforms, although similar in their peak value of 5.17

Amps, show that the diode conducts more current under the lighter loaded condition of

45.15 $\Omega$. Figure 5.4 shows that the increase in capacitance increases the inductor

current from 5.17 to 7.56 Amps, broadens the resonant frequency from 86.5 to 91 Hz,

and increases the output voltage from 125 to 151.5 Volts rms. In that the change in the

$f_r/f_o$ ratio is rather small, a negligible change in distortion is observed. With an increase

in load inductance, the expected result is a slight decrease in output voltage and

inductor current. Figure 5.5 verifies the expected output waveforms. Figures 5.6, 5.7,

and 5.8 are the PSpice simulations with the same changes in R, C, and L. In

comparison with Figure 4.5, the waveforms are not as accurate as the laboratory test

studies for changes in load capacitance and load inductance. Figure 5.7 does not clearly

show the increase in output voltage and resonant frequency. Likewise, Figure 5.8 does

not show the slight decreases in output voltage and inductor current.

## E. CONCLUSION

In the construction of the center-tapped supply Mapham converter in the Power Systems laboratory, hardware values were within 10% of design specifications. This close relation to the theoretical provided excellent test results. The test studies showed that there are still instances where PSpice computer simulation is not a viable substitute for laboratory testing. Resolution of the identified laboratory implementation issues will allow for test studies of the converter at much higher frequencies.

50

## VARIABLE AC/DC POWER SUPPLY
## MODEL # P102-PC
## IP # 41002
## PARTS LIST

| Item No. | Item Label | Qty. | Description | Manufacturer | Manufacturer Part # | IP Part # |
|---|---|---|---|---|---|---|
| 1 | EN1 | 1 | Enclosure 24" x 14l" x 13" As per Dwg. # EN13176 | Hammond | S-80700 | EN13176 |
| 2 | | 1 | Front Panel: Arboron 1/4" x 12-59/64" x 22-59/64" As per Dwg. P102-PC, Sheet # 1 | | | BD10662-A |
| 3 | F1,2,3 | 3 | Input Fuses, 50A, 600V Type 4 | Gould | A60X50 | FU13613 |
| 4 | FHDR | 3 | Fuse Holders for Input Fuses | Inverpower | | FG31013 |
| 5 | | 6 | Heatsinks Aluminum Extrusion 6 - 4" x 4" x 3" lg | Aaall Aarex | 61270 4G4 | |
| 6 | Q1 to Q6 | 6 | Thyristors, 1/2" - 20 Stud | | | |
| | | | 75A, 1200V | Westcode | P080PH12-FHD | TY19126 |
| | | | 85A, 1500V | Westcode | N086PH15 | TY18986 |
| 7 | L1 to L6 | 12 | di/dt Inductors 1-9/16" OD x 15/16" ID x 9/16" | Arnold Engineering | A254168-Z-GR | FE12453 |
| 8 | RS1-RS6 CS1-CS6 | 1 | Device Snubbers Located on PRC-1A Snubber Board R - 15$\Omega$, 12W Non-Inductive C - 0.22$\mu$f, 480V | Inverpower | PRC-1A | FG30044 |
| 9 | PPT-2A | 1 | Six Channel Pulse Transformer Card | Inverpower | PPT-2ALAB | FG30094 |
| 10 | | 10 | Knurled Knob and Terminal Post Assembly | | | FG41050 |
| 11 | | 6 | Panel Mount Phone Jacks for Thyristor Gating Signals | Armaco | DD1300-8 (D142) | CO12332 |

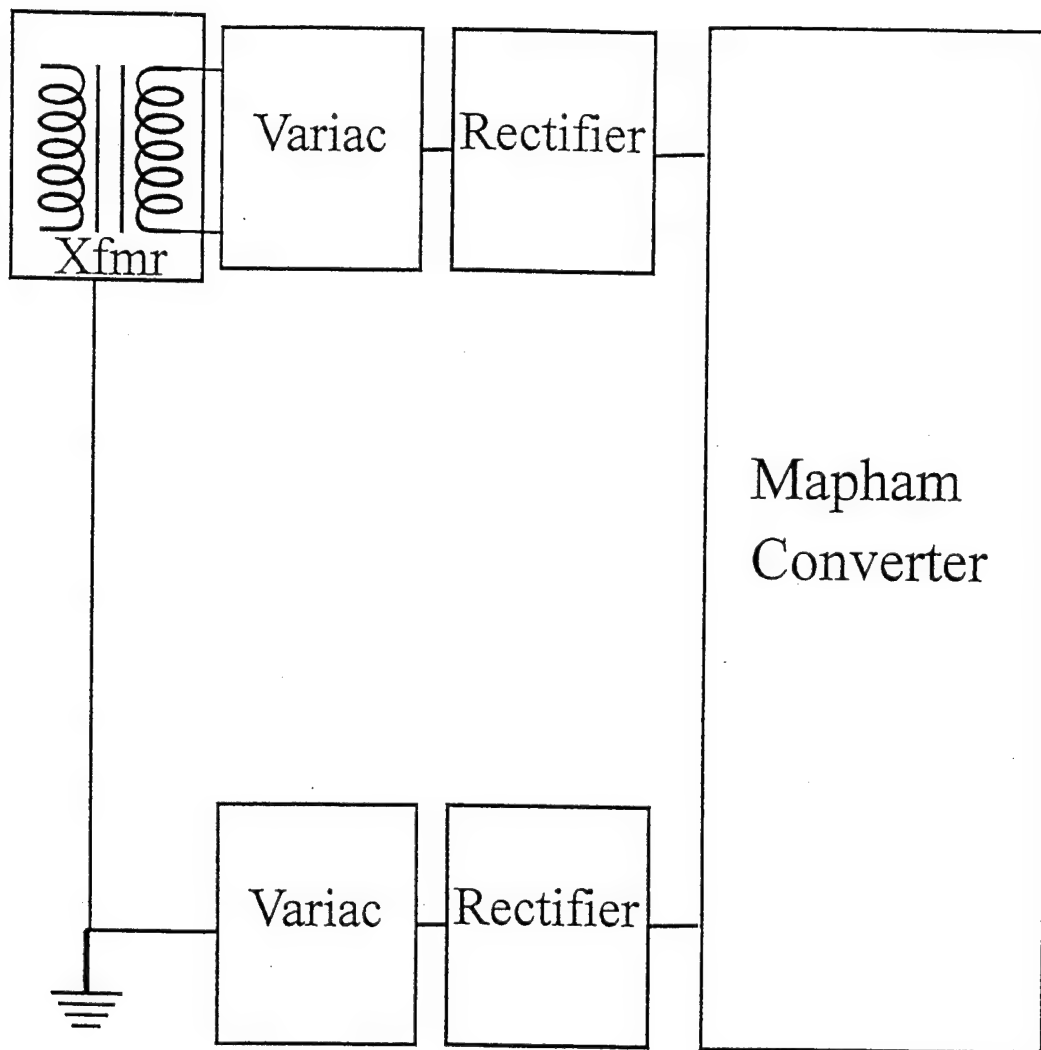Figure 5.1     Variable AC/DC Power Supply Parts List

51

# Mapham Converter



Figure 5.2    Construction of Two DC Sources for the Mapham Converter
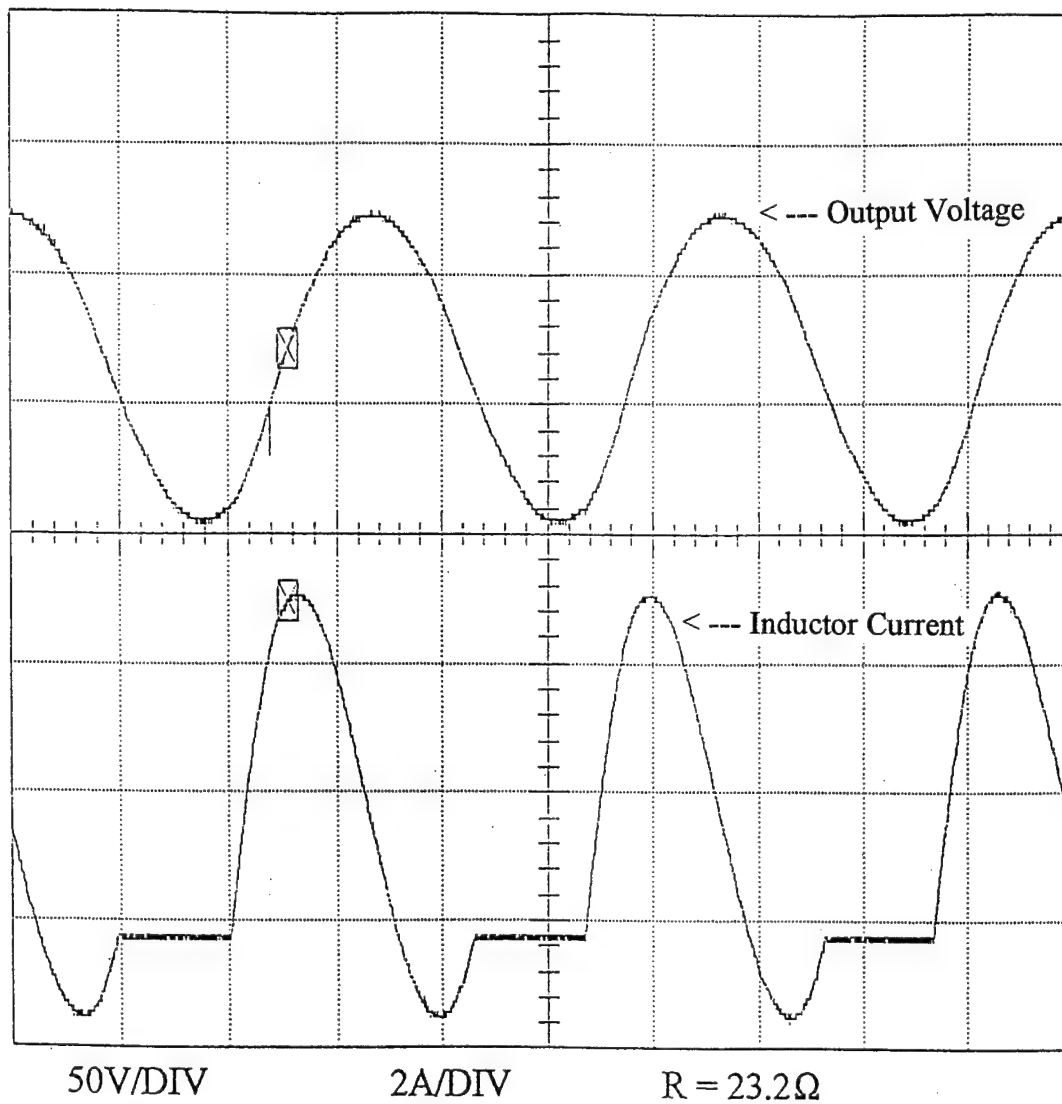
Figure 5.3    Oscilloscope Waveforms of Load Resistance Variation (R = 23.2Ω)

<--- Output Voltage

<--- Inductor Current

50V/DIV　　　2A/DIV　　　$C = 700\mu F$
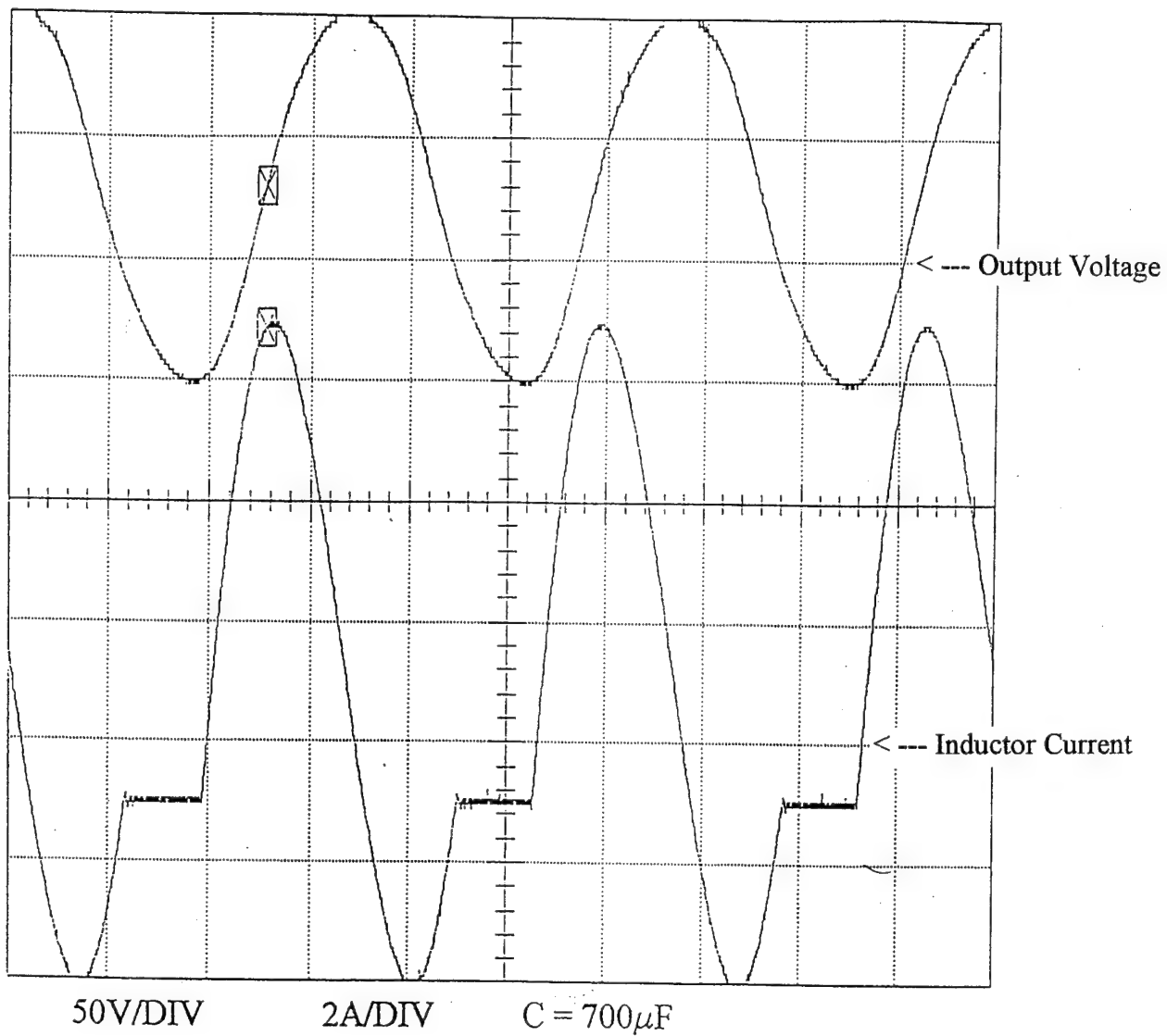
Figure 5.4　Oscilloscope Waveforms of Load Capacitance Variation ($C = 700\mu F$)

54

50V/DIV        2A/DIV        L = 12.75mH

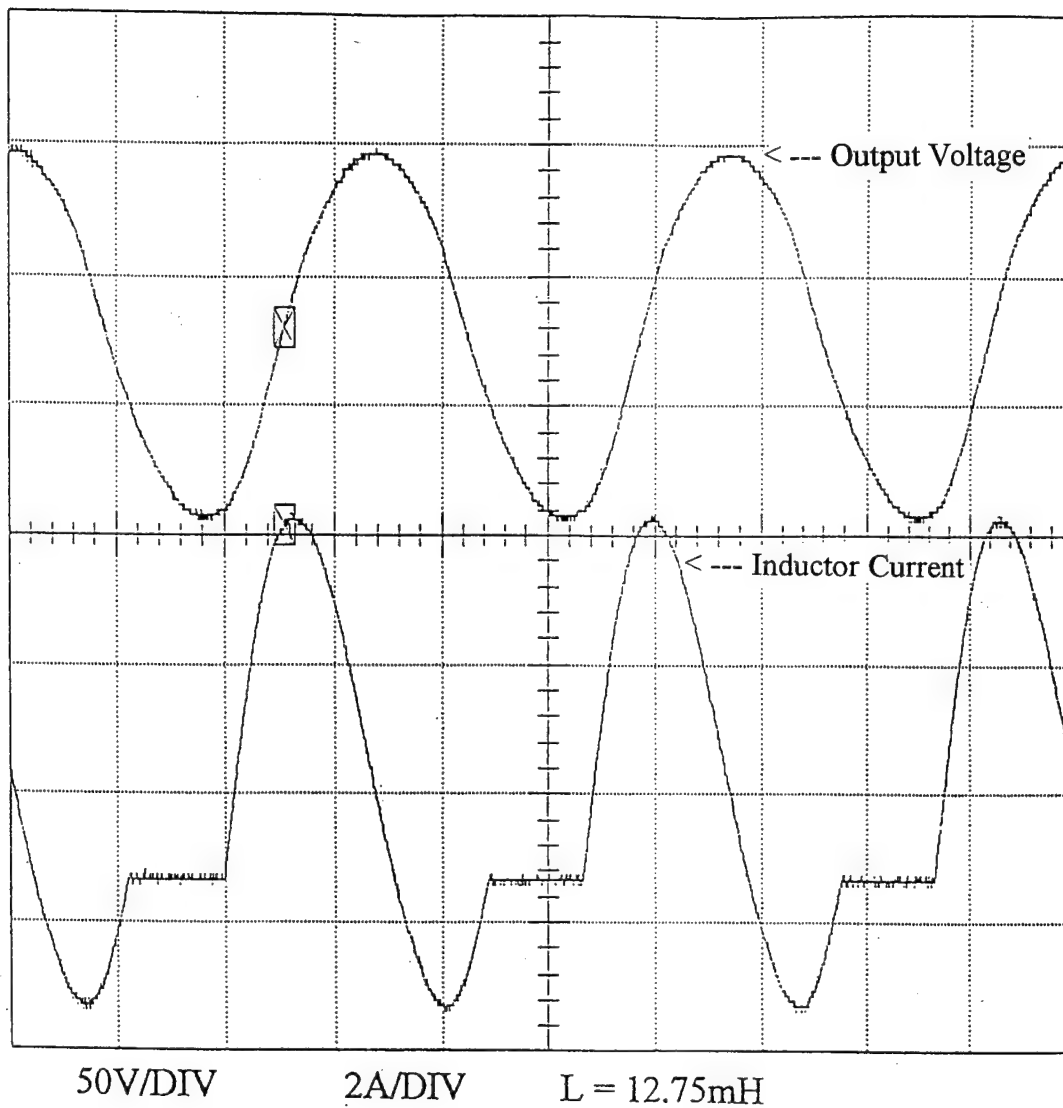Figure 5.5    Oscilloscope Waveforms of Load Inductance Variation (L = 12.75mH)
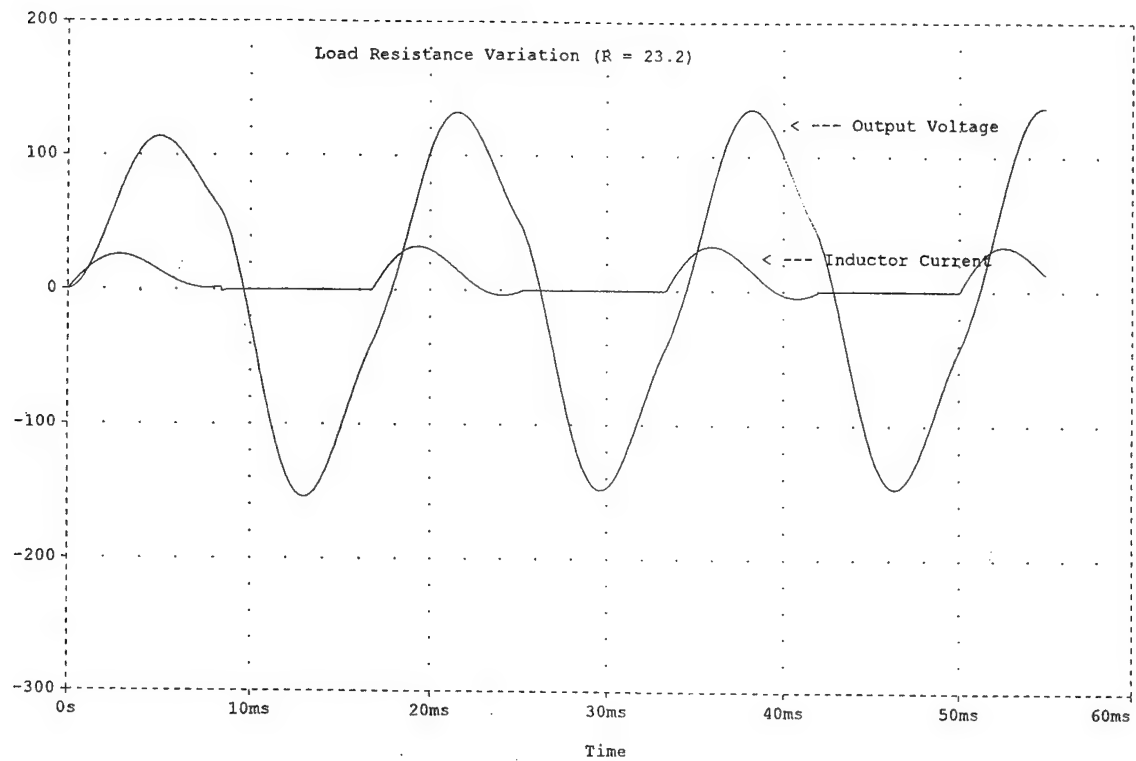
Figure 5.6    PSpice Simulation of Load Resistance Variation (R = 23.2Ω)

56

PSpice Test Study - Load Capacitance Variation (C = 700uF)

<-- Output Voltage

<-- Inductor Current

Time

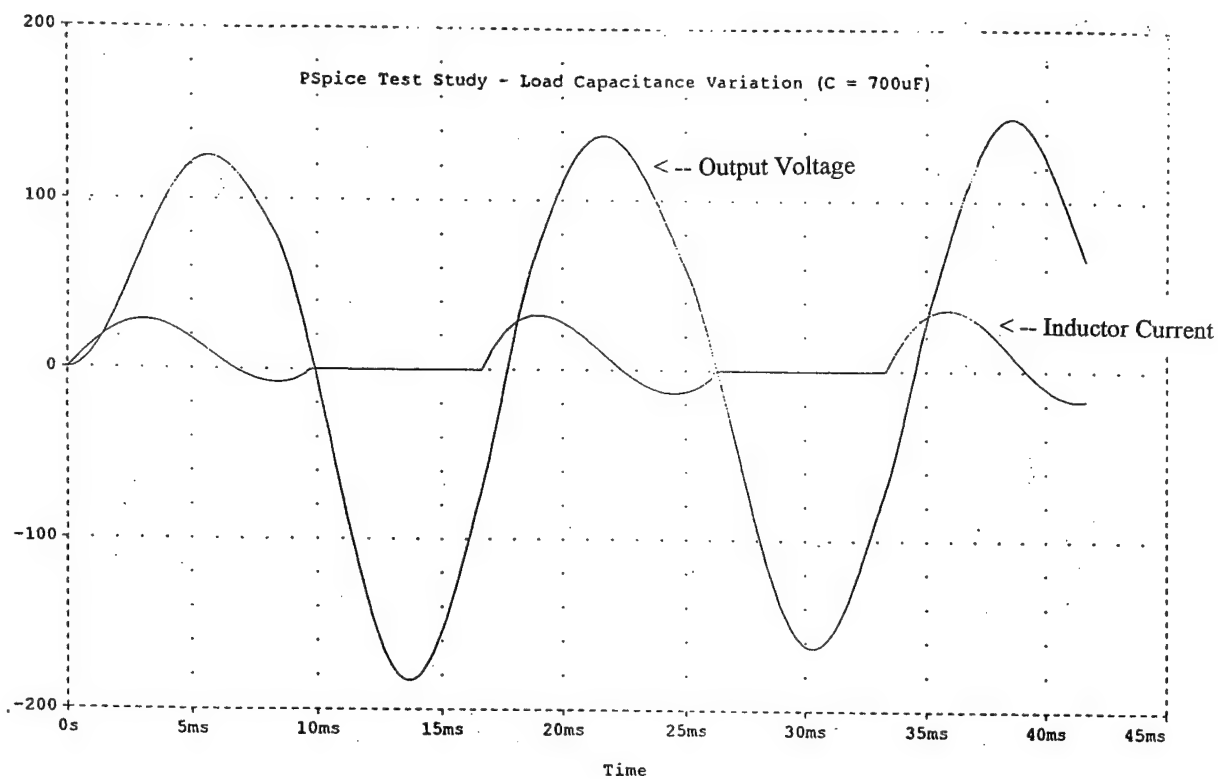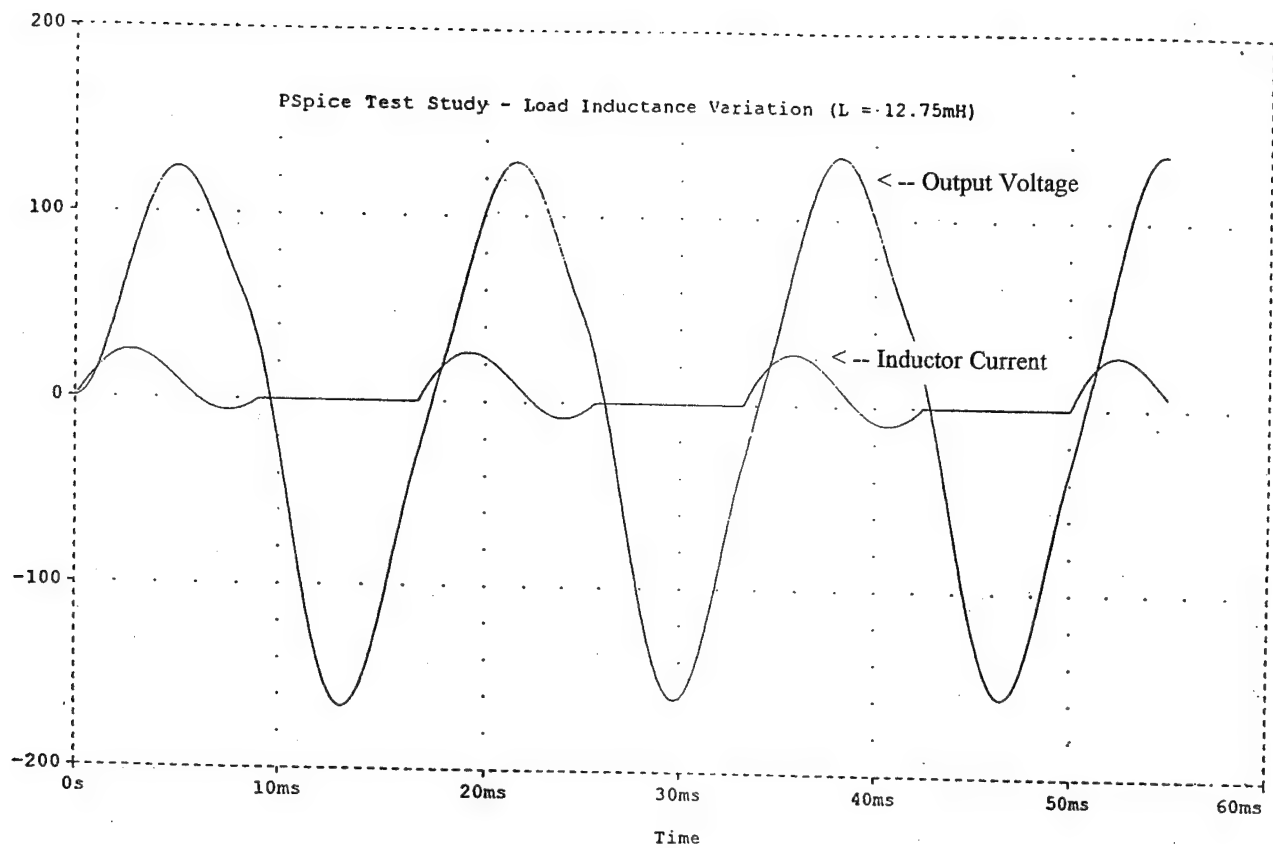Figure 5.7    PSpice Simulation of Load Capacitance Variation (C = 700$\mu$F)

57

Figure 5.8    PSpice Simulation of Load Inductance Variation (L = 12.75mH)

# VI. SERIES-CONNECTED MAPHAM CONVERTER BY TRANSFORMER

## A. INTRODUCTION

This chapter presents information concerning the series connection of the

Mapham bridge configuration through an isolation transformer. The circuit topology,

operation and voltage control are discussed. Furthermore, PSpice implementation of

the circuit is introduced and implementation issues are detailed. The chapter is

concluded with a look at prospective future research efforts.

## B. SERIES-CONNECTED MAPHAM BRIDGES

An electrical schematic of the series-connected Mapham bridge converter

(SCMB) is given in Figure 6.1. Differences between this bridge converter and the

original, Figure 4.8, include the series capacitance 2C3 and the isolation transformer.

The series capacitance protects the converter from a short circuit on the high-frequency

link and the transformer is needed to account for mutual inductance between the two

Mapham bridges.

In order to explain the operation of the source converter the top bridge converter

in Figure 6.1 is considered. The switches in the bridge consist of a thyristor and a

flyback diode. The thyristors T1 and T2 are gated on together as is the pair T3 and T4.

The gate logic signals for the top and bottom bridges are given in Figure 6.2. As

shown, the gate logic signal for the $T_{12}$ pair is displaced $\pi$ radians from the $T_{34}$ pair

signal. The duration of the gate signal is assumed to be sufficient to guarantee that the

device turns on. As the device is a thyristor, it remains on until the current goes to zero. The firing and current flow aspect of the bridge is the same as the original Mapham bridge aforementioned in Chapter II.

In that the top and bottom bridge converters are series connected through an isolation transformer, the converters are thus forced to interact and several modes of operation are likely to occur; four valves conducting, six valves conducting, or eight valves conducting. A valve being either a thyristor or a flyback diode. A functional representation of the SCMB converter is given in Figure 6.3 illustrating that the output voltages of the bridge converters add in series. The inductance L1 may represent stray inductance or the leakage inductance of the transformer.

Voltage control of the SCMB is accomplished by phase displacing the gating signals of the top and bottom bridge converters. The phase displacement is illustrated in Figure 6.2 and the resultant phasor diagram is given in Figure 6.4. The angle $\phi$ is the angle in which the thyristor pair gate firing of the top converter differs from the thyristor pair gate firing of the bottom converter.

By controlling $\phi$, the magnitude of the high-frequency link voltage may be controlled. As $\phi$ is increased, the link voltage will decrease. [Ref. 4, p. 7-11]

## C. PSPICE IMPLEMENTATION

With the extreme difficulty of synchronizing four thyristors in the laboratory, the SCMB, like the original Mapham bridge, was constructed in PSpice for analysis via

computer simulation. The SCMB was constructed with the parameters specified in Table 6.1.

<u>Series Connected Mapham Bridge Parameters</u>

| C1 = 1.40 μF | C2 = 1.40 μF | C3 = 1.25 μF | Lm = 24.0 μH | fo = 20 kHz |
|---|---|---|---|---|

Table 6.1

<u>IMPLEMENTATION ISSUES</u>

All efforts to simulate this circuit at various frequencies in PSpice were unsuccessful. Convergence errors occurred from simulation of frequencies ranging from 60 Hz to 1 kHz. Errors in PSpice of this type indicate that the flyback diodes are not turning-on properly. Selection of various diodes in the Model Library produced no change in simulation results. MicroSim expert, Brian Hirasuna, was contacted, but he, too, was unable to resolve the issue.

## D. FUTURE RESEARCH

With the difficulty of pulse synchronization in the laboratory and the experienced difficulty of simulation in PSpice, future research can be conducted via another software package (i.e. ACSL). The researcher will require requisite knowledge on phase-controlled series-parallel resonant converters.

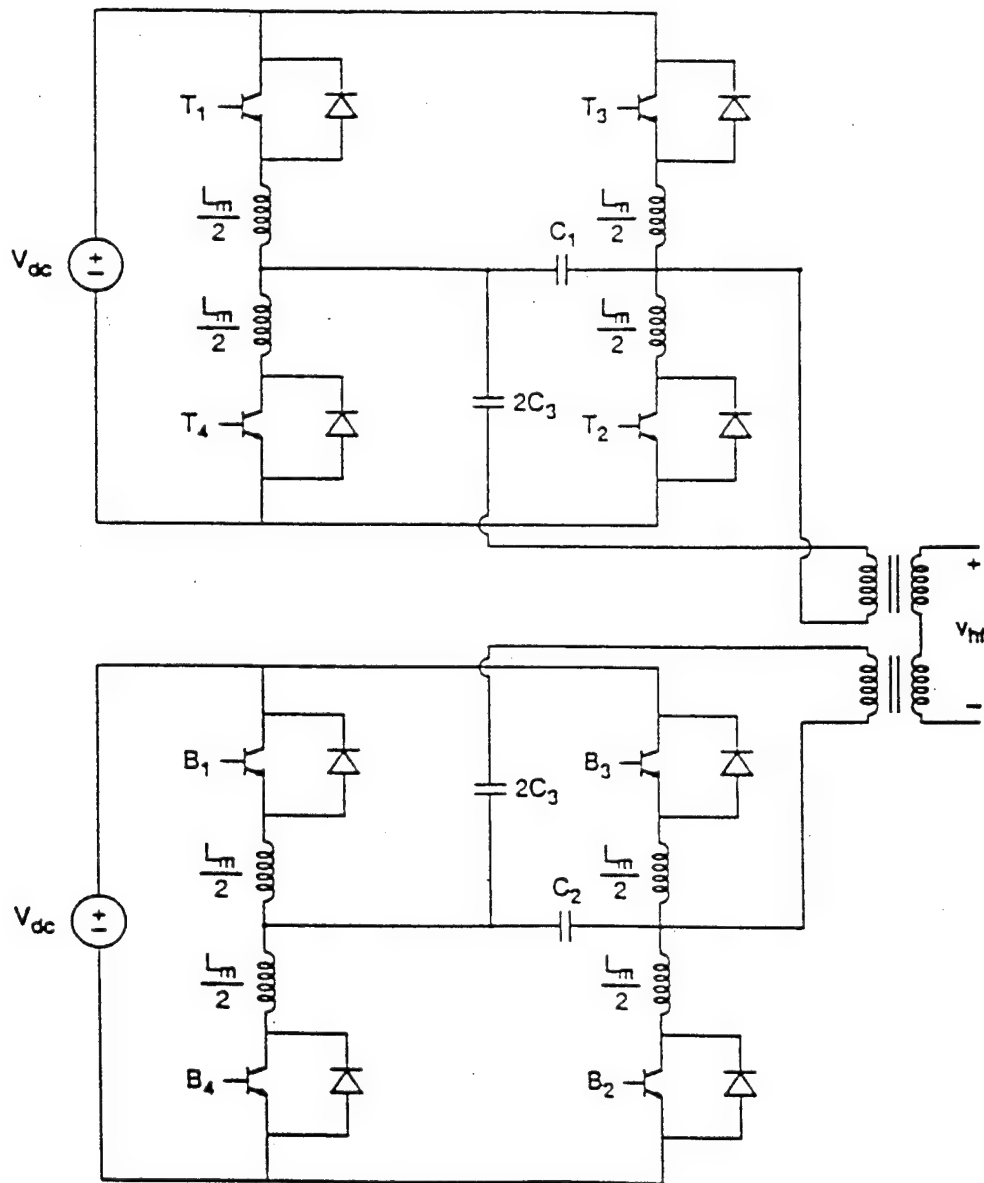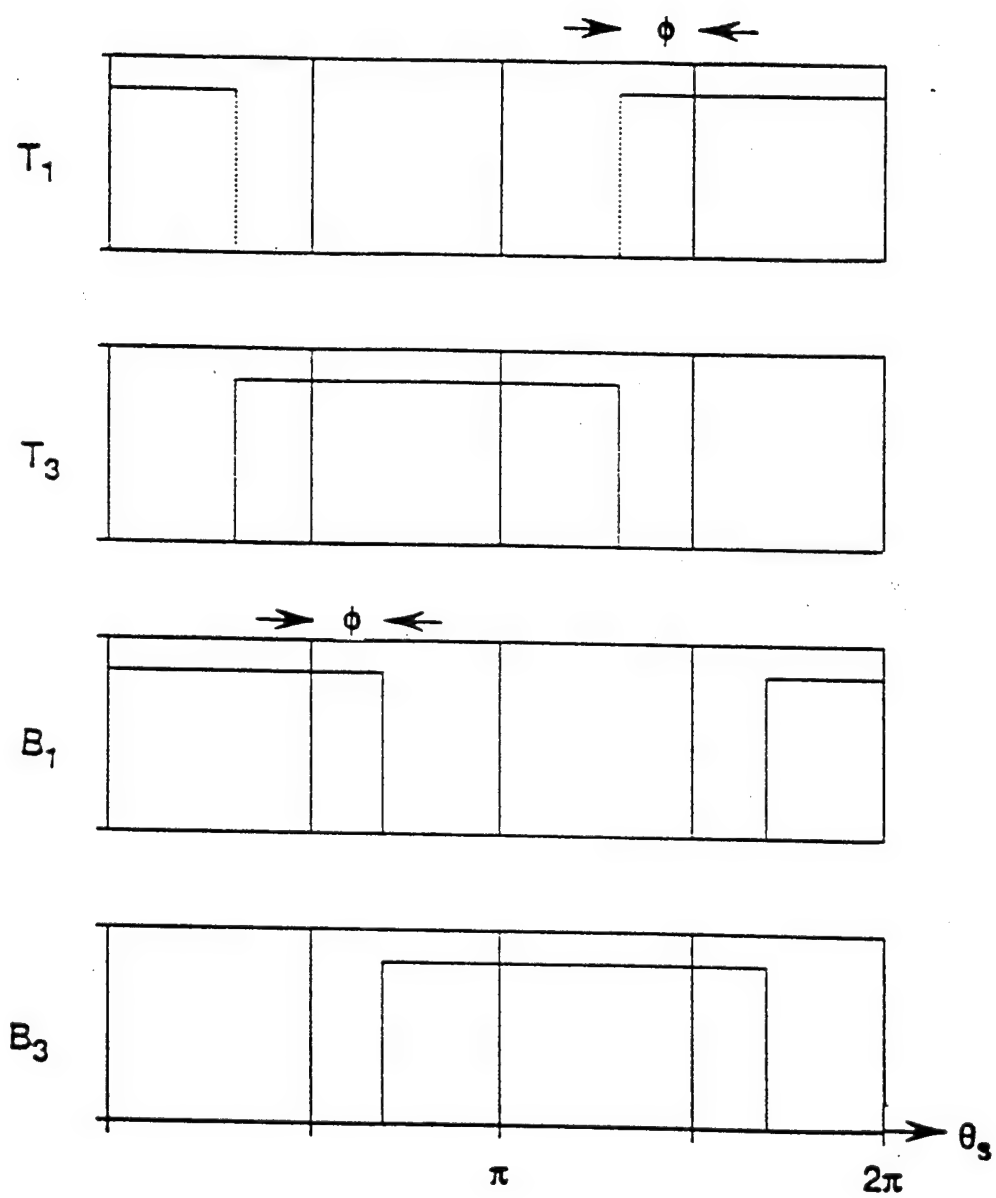Figure 6.1    Series-Connected Mapham Bridge Configuration Through a Transformer

62

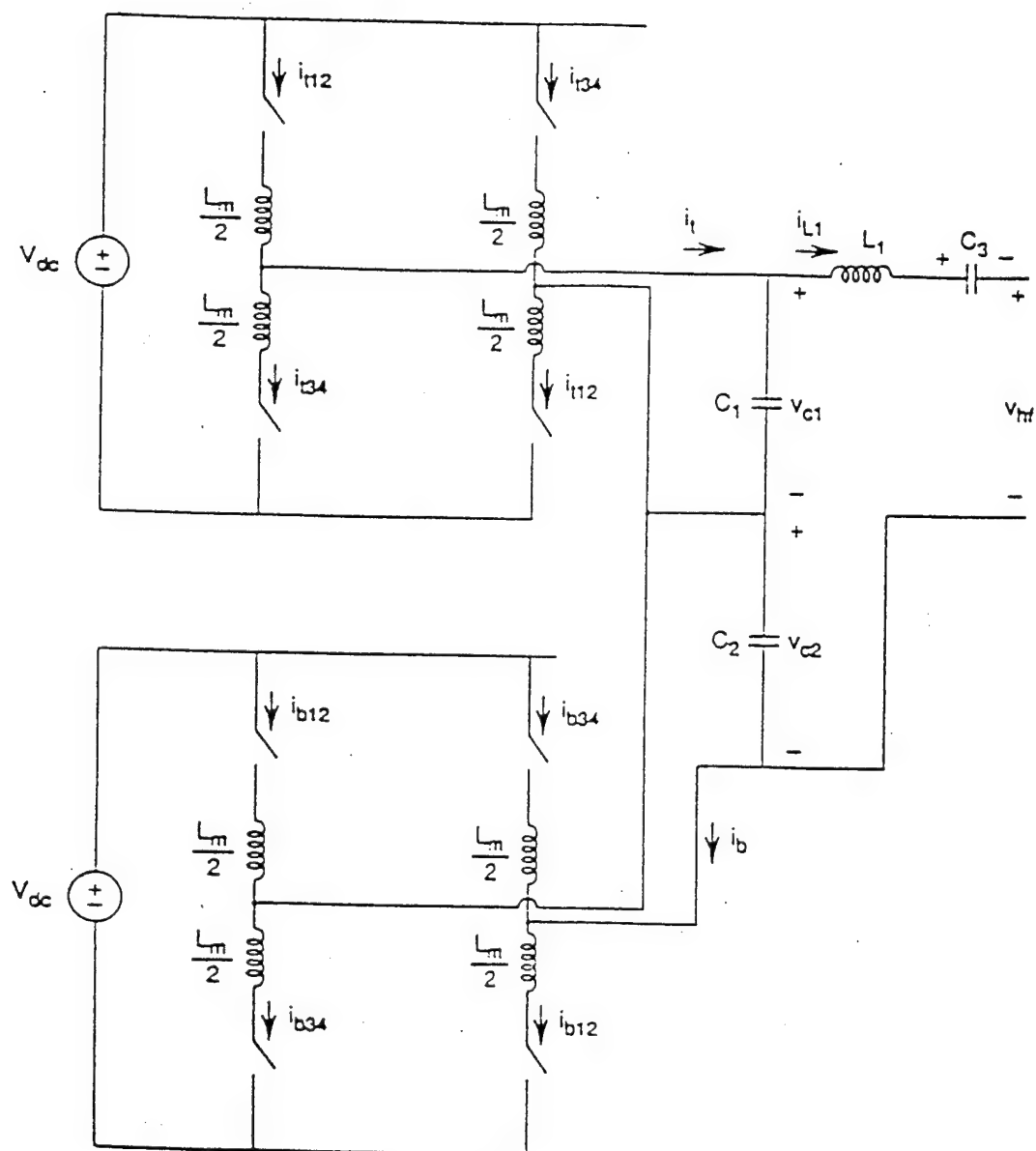Figure 6.2    Gate Logic Signals for the SCMB

63

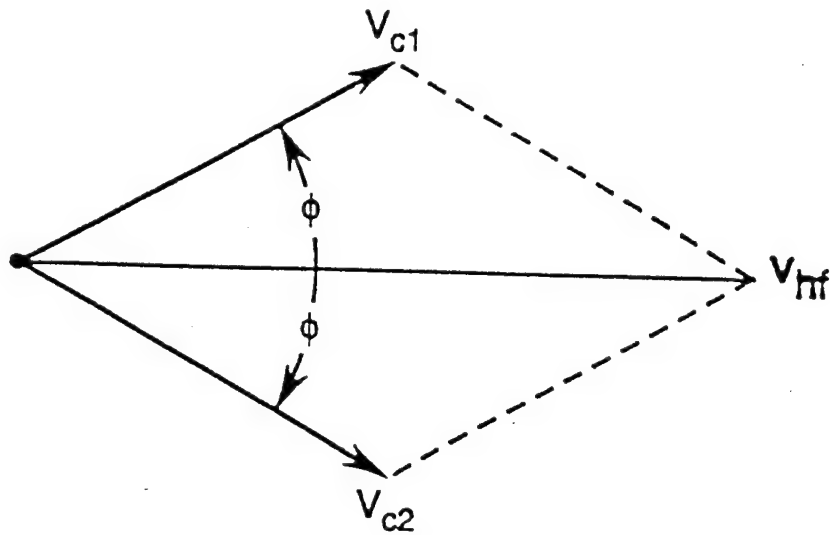Figure 6.3    Network Representation of the SCMB

64

Figure 6.4     Phasor Diagram of the SCMB Output Voltages

# VII. CONCLUSIONS

The Mapham converter is a parallel output resonant converter. Its capabilities include high-frequency operation with near-zero switching losses, small volume and weight of components, and high efficiency. The converter was analyzed, simulated, and designed to provide a new approach to reducing the weight and size and cost of many DoD systems. Although the higher-frequency operation of the Mapham converter was not achieved, the remaining objectives were demonstrated in this research effort. An analytical representation of the Mapham converter was developed for both the center-tapped and bridge configurations. A PSpice model of the converter was designed, simulation of the model was demonstrated, and validation against hardware implementation was conducted. A Mapham converter test bed was built in the Power Systems Laboratory and several studies were performed to evaluate the performance of the circuit.

The equipment available in the Power Systems Laboratory is limited in its ability to realize high-frequency switching circuits. As a consequence, circuit testing was constrained to the 60 Hertz range despite the obvious utility of higher frequency converters. In order for the gate pulses to be properly synchronized at higher frequencies, the researcher will need to specially design the firing circuitry for the thyristors. Future research will require requisite knowledge to handle the issues associated with electrically isolated firing circuits for the thyristors.

Dr. Mapham's work furthered the advancement of resonant converter technology in today's rapidly changing environment of power electronics, but the upper frequency limits of his converter remain undetermined. Continued research will undoubtedly result in smaller, lighter, less expensive, and more reliable power systems.

# APPENDIX A  MAPHAM CONVERTER DESIGN TABLE

The table in this appendix is needed for design of the Mapham converter configurations.

TABLE A.1  Mapham Converter Design Table ($L_2/L = 20$)

69

# TABLE A.1

## MAPHAM CONVERTER DESIGN DATA

$$L_2/L = 20$$

| $\dfrac{f_r}{f_o}$ | $\dfrac{R}{\sqrt{L/C}}$ | $\dfrac{I_S\sqrt{L/C}}{E}$ | $\dfrac{I_D\sqrt{L/C}}{E}$ | $\dfrac{I_{DC}\sqrt{L/C}}{E}$ | $\dfrac{V_C}{E}$ | $\dfrac{V_{C\,rms}}{E}$ | $\dfrac{V_S}{E}$ | $\dfrac{t_S}{\pi\sqrt{LC}}$ | $\dfrac{t_D}{\pi\sqrt{LC}}$ | $\dfrac{t_{min}}{\pi\sqrt{LC}}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| | 3 | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ |
| | 5 | 0.77 | 0.24 | 0.071 | 1.54 | 0.85 | 2.54 | 1.10 | 0.64 | 0.50 |
| | 10 | 0.70 | 0.43 | 0.037 | 1.61 | 0.86 | 2.65 | 1.00 | 0.80 | 0.70 |
| 3 | 20 | 0.65 | 0.52 | 0.018 | 1.63 | 0.86 | 2.78 | 0.94 | 0.86 | 0.76 |
| | 50 | 0.61 | 0.56 | 0.007 | 1.63 | 0.86 | 2.90 | 0.92 | 0.90 | 0.80 |
| | 100 | 0.59 | 0.58 | 0.003 | 1.62 | 0.86 | 2.90 | 0.90 | 0.92 | 0.82 |
| | 3 | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ |
| | 5 | 1.13 | 0.44 | 0.127 | 1.83 | 1.13 | 2.87 | 1.08 | 0.72 | 0.50 |
| | 10 | 1.05 | 0.64 | 0.066 | 1.90 | 1.15 | 2.90 | 1.02 | 0.82 | 0.70 |
| 2 | 20 | 1.07 | 0.77 | 0.034 | 1.97 | 1.18 | 2.89 | 1.00 | 0.84 | 0.76 |
| | 50 | 1.08 | 0.89 | 0.014 | 2.03 | 1.21 | 2.87 | 0.98 | 0.88 | 0.80 |
| | 100 | 1.11 | 0.97 | 0.007 | 2.09 | 1.23 | 2.86 | 0.96 | 0.90 | 0.82 |
| | 3 | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ |
| | 5 | 1.30 | 0.60 | 0.189 | 2.00 | 1.38 | 3.31 | 1.04 | 0.70 | 0.44 |
| | 10 | 1.15 | 0.80 | 0.086 | 2.03 | 1.39 | 3.37 | 0.96 | 0.80 | 0.62 |
| 1.5 | 20 | 1.07 | 0.89 | 0.048 | 2.03 | 1.39 | 3.39 | 0.92 | 0.84 | 0.70 |
| | 50 | 1.01 | 0.94 | 0.019 | 2.04 | 1.39 | 3.39 | 0.90 | 0.86 | 0.72 |
| | 100 | 1.00 | 0.96 | 0.009 | 2.03 | 1.39 | 3.39 | 0.90 | 0.86 | 0.74 |
| | 3 | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ |
| | 5 | 1.47 | 0.70 | 0.229 | 2.14 | 1.51 | 3.52 | 1.00 | 0.67 | 0.35 |
| | 10 | 1.30 | 0.92 | 0.117 | 2.16 | 1.53 | 3.63 | 0.92 | 0.77 | 0.55 |
| 1.35 | 20 | 1.21 | 1.02 | 0.059 | 2.17 | 1.53 | 3.68 | 0.88 | 0.81 | 0.61 |
| | 50 | 1.16 | 1.08 | 0.023 | 2.17 | 1.53 | 3.72 | 0.86 | 0.83 | 0.65 |
| | 100 | 1.14 | 1.10 | 0.012 | 2.17 | 1.53 | 3.73 | 0.86 | 0.83 | 0.67 |
| | 3 | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ |
| | 5 | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ |
| | 10 | 1.55 | 1.02 | 0.151 | 2.39 | 1.74 | 3.91 | 0.88 | 0.72 | 0.42 |
| 1.2 | 20 | 1.45 | 1.16 | 0.076 | 2.39 | 1.75 | 4.00 | 0.84 | 0.76 | 0.50 |
| | 50 | 1.40 | 1.25 | 0.030 | 2.39 | 1.74 | 4.06 | 0.82 | 0.78 | 0.52 |
| | 100 | 1.37 | 1.29 | 0.015 | 2.41 | 1.76 | 4.08 | 0.82 | 0.78 | 0.54 |
| | 3 | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ |
| | 5 | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ |
| | 10 | 1.83 | 1.06 | 0.195 | 2.66 | 1.97 | 4.11 | 0.86 | 0.68 | 0.32 |
| 1.1 | 20 | 1.72 | 1.24 | 0.098 | 2.67 | 1.98 | 4.23 | 0.82 | 0.72 | 0.40 |
| | 50 | 1.64 | 1.35 | 0.039 | 2.67 | 1.98 | 4.31 | 0.80 | 0.74 | 0.44 |
| | 100 | 1.62 | 1.38 | 0.019 | 2.68 | 1.98 | 4.34 | 0.78 | 0.76 | 0.46 |

Δ Signifies no turn-off time for one or more cycles from start up. [Ref. 1]

# LIST OF REFERENCES

Mapham, N., "An SCR With Good Regulation and Sine-Wave Output," in *IEEE Transaction Industry and General Applications,* April 1967.

Wood, P., *Switching Power Converters,* Robert E. Krieger Publishing, Malabar, FL, 1981.

Kazimierczuk, M.K., Thirunarayan, N. and Wang, S., "Analysis of Series-Parallel Resonant Converter," in *IEEE Transactions On Aerospace And Electronic Systems,* January 1993.

Ciezki, J. G., *The Analysis and Reduced-Order Modeling of a Proposed Aerospace Electric Drive,* Ph.D. Dissertation, Purdue University, West Lafayette, IN, 1993.

Tuinenga, P. W., *A Guide To Circuit Simulation & Analysis Using PSpice,* Prentice-Hall, Englewood Cliffs, NJ, 1992.

MicroSim Corporation, *Circuit Analysis User's Guide Using Schematics,* Irvine, CA, 1995.

# INITIAL DISTRIBUTION LIST

No. of Copies

1. Defense Technical Information Center 2
   8725 John J. Kingman Rd., STE 0944
   Ft. Belvoir, VA 22060-6218

2. Library Code 013 2
   Naval Postgraduate School
   Monterey, CA 93943-5101

3. Chairman, Code EC 1
   Department of Electrical and Computer Engineering
   Naval Postgraduate School
   Monterey, CA 93943-5121

4. Professor John Ciezki, Code EC/Cy 1
   Department of Electrical and Computer Engineering
   Naval Postgraduate School
   Monterey, CA 93943-5121

5. Professor Robert Ashton, Code EC/Ah 1
   Department of Electrical and Computer Engineering
   Naval Postgraduate School
   Monterey, CA 93943-5121

6. LT Jerry Tyner 1
   201 Glenwood Circle
   Apt. 17D
   Monterey, CA 93940